



## IGLOO® 2 Automotive Grade 1 AC/DC Electrical Characteristics

Microchip's automotive grade IGLOO® 2 FPGAs offer the best-in-class security, industry leading high reliability and lowest static power in a flash-based fabric. With a strong heritage of supplying to Military and Aviation customers, Microchip automotive grade devices are ideally suited to meet the demands of the automotive industry providing the lowest total-cost-of-ownership. These next-generation devices integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, and multiple embedded memory blocks on a single chip with extended temperature support.

Automotive grade IGLOO 2 devices offer up to 90 K logic elements, up to 5 MB of embedded RAM with on-chip flash, 32 kbyte embedded SRAM, and multiple DMA controllers. IGLOO 2 FPGAs are the best alternative to ASICs and SRAM based FPGAs with their advantages of Zero FIT reliability, tamper-free advanced security, industry's lowest static power and supply assurance for long product lifetime support.

### Device Status

The following IGLOO 2 devices are available.

**TABLE 1: IGLOO® 2 FPGA DEVICE STATUS**

| Design Security Device Densities | Status     |
|----------------------------------|------------|
| 005                              | Production |
| 010                              | Production |
| 025                              | Production |
| 060                              | Production |
| 090                              | Production |

### Pin Descriptions

The pin descriptions are published separately:

**Note 1:** [DS0124: IGLOO2 Pin Descriptions](#)

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# Contents

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|  |    |
|--|----|
| Introduction .....   | 1  |
| 1.0 General Specifications .....                                     | 4  |
| 1.1 Operating Conditions .....                                       | 4  |
| 1.2 Overshoot/Uundershoot Limits .....                               | 7  |
| 1.3 Thermal Characteristics .....                                    | 7  |
| 1.4 Power Consumption .....  | 8  |
| 1.5 Average Fabric Temperature and Voltage Derating Factors .....    | 10 |
| 1.6 Timing Model .....   | 11 |
| 2.0 User I/O Characteristics .....                                   | 13 |
| 2.1 Input Buffer and AC Loading .....                                | 13 |
| 2.2 Output Buffer and AC Loading .....                               | 13 |
| 2.3 Tristate Buffer and AC Loading .....                             | 14 |
| 2.4 I/O Speeds .....   | 15 |
| 2.5 Detailed I/O Characteristics .....                               | 16 |
| 2.6 Single-Ended I/O Standards .....                                 | 17 |
| 2.7 Voltage Referenced I/O Standards .....                           | 32 |
| 2.8 Differential I/O Standards .....                                 | 42 |
| 2.9 I/O Register Specifications .....                                | 51 |
| 2.10 DDR Module Specification .....                                  | 54 |
| 3.0 Logic Element Specifications .....                               | 60 |
| 3.1 4-input LUT (LUT-4) .....  | 60 |
| 3.2 Sequential Module .....  | 61 |
| 4.0 Global Resource Characteristics .....                            | 63 |
| 5.0 FPGA Fabric SRAM .....   | 65 |
| 5.1 FPGA Fabric Large SRAM (LSRAM) .....                             | 65 |
| 5.2 FPGA Fabric Micro SRAM (uSRAM) .....                             | 71 |
| 6.0 Switching Characteristics .....                                  | 79 |
| 6.1 Embedded NVM (eNVM) Characteristics .....                        | 79 |
| 6.2 Crystal Oscillator .....   | 79 |
| 6.3 On-Chip Oscillator .....   | 80 |
| 6.4 Clock Conditioning Circuits (CCC) .....                          | 81 |
| 6.5 JTAG .....   | 84 |
| 6.6 Power-up to Functional Times .....                               | 85 |
| 6.7 DEVRST_N Characteristics .....                                   | 86 |
| 6.8 DEVRST_N to Functional Times .....                               | 87 |
| 6.9 System Controller SPI Characteristics .....                      | 88 |
| 6.10 Mathblock Timing Characteristics .....                          | 89 |
| 6.11 Flash*Freeze Timing Characteristics .....                       | 91 |
| 6.12 IGLOO 2 Specifications .....                                    | 91 |
| 6.13 HPMs Clock Frequency .....                                      | 91 |
| 6.14 IGLOO 2 Serial Peripheral Interface (SPI) Characteristics ..... | 92 |
| 6.15 SRAM PUF .....  | 94 |
| 6.16 Non-deterministic Random Bit Generator Characteristics .....    | 95 |
| 6.17 Cryptographic Block Characteristics .....                       | 95 |
| Appendix A: Revision History .....                                   | 97 |
| The Microchip WebSite .....  | 98 |
| Customer Change Notification Service .....                           | 98 |
| Customer Support .....   | 98 |

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## 1.0 GENERAL SPECIFICATIONS

### 1.1 Operating Conditions

Stresses beyond those listed in the following table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table is not implied.

TABLE 1-1: ABSOLUTE MAXIMUM RATINGS

| Symbol              | Parameter   | Limits |      | Units | Notes |
|---------------------|---|--------|------|-------|-------|
|                     |   | Min    | Max  |       |       |
| VDD                 | DC core supply voltage. Must always power this pin.   | -0.3   | 1.32 | V     | —     |
| VPP                 | Power supply for charge pumps (for normal operation and programming). Must always power this pin. | -0.3   | 3.63 | V     | —     |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0-5   | -0.3   | 3.63 | V     | —     |
| VDDIx               | DC FPGA I/O buffer supply voltage for MSIO I/O Bank   | -0.3   | 3.63 | V     | —     |
|                     | DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks                                       | -0.3   | 2.75 | V     | —     |
| VI                  | I/O Input voltage for MSIO I/O Bank   | -0.3   | 3.63 | V     | —     |
|                     | I/O Input voltage for MSIOD/DDRIO I/O Bank  | -0.3   | 2.75 | V     | —     |
| VPPNVM              | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.        | -0.3   | 3.63 | V     | —     |
| T <sub>STG</sub>    | Storage temperature   | -65    | 150  | °C    | *     |
| T <sub>J</sub>      | Junction temperature  | —      | 145  | °C    | —     |

**Note:** \* For flash programming and retention maximum limits, see [Table 1-3](#). For recommended operating conditions, see [Table 1-2](#).

The following table lists the recommended operating conditions.

TABLE 1-2: RECOMMENDED OPERATING CONDITIONS

| Symbol              | Parameter   | Conditions         | Min   | Typ | Max   | Units | Notes |
|---------------------|---|--------------------|-------|-----|-------|-------|-------|
| T <sub>J</sub>      | Operating Junction Temperature  | Automotive Grade 1 | -40   | 25  | 135   | °C    | —     |
|                     | Programming Junction Temperature  | —                  | 0     | 25  | 85    | °C    | —     |
|                     |   | —                  | -40   | 25  | 100   | °C    | 1     |
| VDD                 | DC core supply voltage. Must always power this pin.   | —                  | 1.14  | 1.2 | 1.26  | V     | —     |
| VPP                 | Power Supply for Charge Pumps (for Normal Operation and Programming) for 005, 010, 025, and 060 Devices | 2.5V Range         | 2.375 | 2.5 | 2.625 | V     | —     |
|                     |   | 3.3V Range         | 3.15  | 3.3 | 3.45  | V     | —     |
|                     | Power Supply for Charge Pumps (for Normal Operation and Programming) for 090 devices                    | 3.3V Range         | 3.15  | 3.3 | 3.45  | V     | —     |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0-5   | 2.5V Range         | 2.375 | 2.5 | 2.625 | V     | —     |
|                     |   | 3.3V Range         | 3.15  | 3.3 | 3.45  | V     | —     |

**TABLE 1-2: RECOMMENDED OPERATING CONDITIONS (CONTINUED)**

| Symbol | Parameter   | Conditions    | Min           | Typ          | Max           | Units | Notes |
|--------|---|---------------|---------------|--------------|---------------|-------|-------|
| VDDIx  | 1.2V DC supply voltage  | —             | 1.14          | 1.2          | 1.26          | V     | —     |
|        | 1.5V DC supply voltage  | —             | 1.425         | 1.5          | 1.575         | V     | —     |
|        | 1.8V DC supply voltage  | —             | 1.71          | 1.8          | 1.89          | V     | —     |
|        | 2.5V DC supply voltage  | —             | 2.375         | 2.5          | 2.625         | V     | —     |
|        | 3.3V DC supply voltage (MSIO only)  | —             | 3.15          | 3.3          | 3.45          | V     | —     |
|        | LVDS differential I/O   | —             | 2.375         | 2.5          | 3.45          | V     | —     |
|        | BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O  | —             | 2.375         | 2.5          | 2.625         | V     | —     |
|        | LVPECL differential I/O   | —             | 3.15          | 3.3          | 3.45          | V     | —     |
| VREFx  | Reference Voltage Supply for DDRIO Banks  | —             | 0.49<br>VDDIx | 0.5<br>VDDIx | 0.51<br>VDDIx | V     | —     |
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP | 2.5V<br>Range | 2.375         | 2.5          | 2.625         | V     | —     |
|        |   | 3.3V<br>Range | 3.15          | 3.3          | 3.45          | V     | —     |

**Note 1:** Programming at this temperature range is available only with VPP in 3.3V range.

**2:** Power supply ramps must all be strictly monotonic, without plateaus.

The following table lists the FPGA operating limits.

**TABLE 1-3: FPGA OPERATING LIMITS**

| Product Grade      | Element | Programming Temperature                                    | Operating Temperature                                      | Programming Cycles | Digest Temperature   | Digest Cycles | Retention (Biased/Unbiased) | Note |
|--------------------|---------|--|--|--------------------|--|---------------|-----------------------------|------|
| Automotive Grade 1 | FPGA    | Min T <sub>J</sub> = 0 °C<br>Max T <sub>J</sub> = 85 °C    | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 135 °C | 500                | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 100 °C | 2000          | 6 Years                     | —    |
|                    |         | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 100 °C | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 135 °C | 500                | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 100 °C | 2000          | 6 Years                     | *    |

**Note:** \* Programming in -40 °C to 100 °C temperature range is available only with VPP in 3.3V range.

The following table lists the embedded FLASH limits.

**TABLE 1-4: EMBEDDED FLASH LIMITS**

| Product Grade      | Element        | Programming Temperature                                    | Maximum Operating Temperature                              | Programming Cycles   | Retention (Biased/Unbiased) |
|--------------------|----------------|--|--|--|-----------------------------|
| Automotive Grade 1 | Embedded flash | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 135 °C | Min T <sub>J</sub> = -40 °C<br>Max T <sub>J</sub> = 135 °C | < 10,000 cycles per pages, up to one million cycles per eNVM array | 6 Years                     |

**Note:** If accelerated programming cycles are required as part of your product qualification, For Reliability report contact Technical Support: <http://www.microchip.com/support>.

The following table lists the device storage temperature and retention.

**TABLE 1-5: DEVICE STORAGE TEMPERATURE AND RETENTION**

| Product Grade | Storage Temperature (T <sub>stg</sub> ) | Retention |
|---------------|---|-----------|
|---------------|---|-----------|

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**TABLE 1-5: DEVICE STORAGE TEMPERATURE AND RETENTION**

|                    |  |         |
|--------------------|--|---------|
| Automotive Grade 1 | Min $T_J = -40^\circ\text{C}$<br>Max $T_J = 135^\circ\text{C}$ | 6 Years |
|--------------------|--|---------|

The following table lists the HTR lifetime.

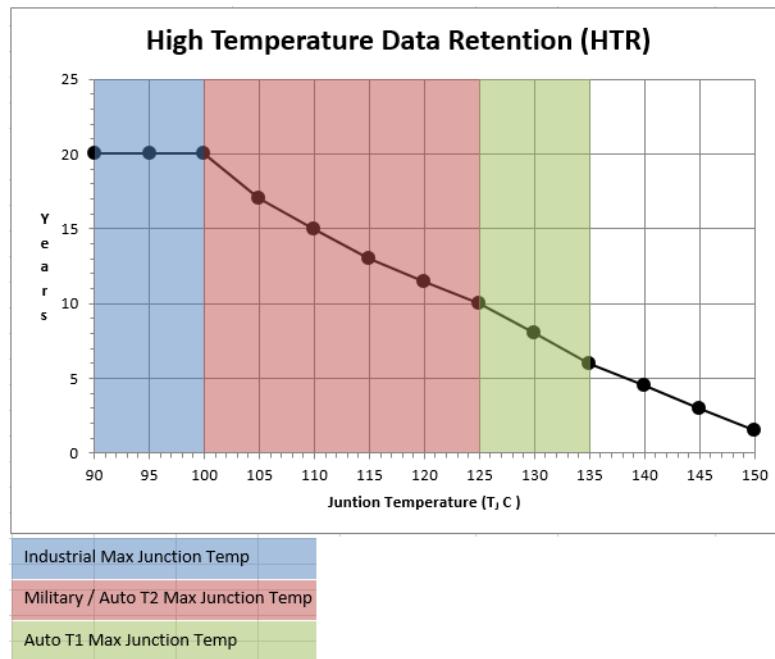
**TABLE 1-6: HIGH TEMPERATURE DATA RETENTION (HTR) LIFETIME**

| $T_J (\text{C})$ | HTR Lifetime* (Years) |
|------------------|-----------------------|
| 90               | 20.0                  |
| 95               | 20.0                  |
| 100              | 20.0                  |
| 105              | 17.0                  |
| 110              | 15.0                  |
| 115              | 13.0                  |
| 120              | 11.5                  |
| 125              | 10.0                  |
| 130              | 8.0                   |
| 135              | 6.0                   |
| 140              | 4.5                   |
| 145              | 3.0                   |
| 150              | 1.5                   |

**Note:** \* HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

**Note:** The IGLOO® 2 Automotive Grade 1 maximum operational junction temperature specification is  $135^\circ\text{C}$ .

The following figure shows the HTR curve.

**FIGURE 1-1: HIGH TEMPERATURE DATA RETENTION (HTR)**

## 1.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to  $-1.0\text{ V}$  for no longer than 10% or the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to  $\text{VCCI} + 1.0\text{ V}$  for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

**Note:** The above specification does not apply to the PCI standard. The IGLOO 2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

## 1.3 Thermal Characteristics

### 1.3.1 INTRODUCTION

The temperature variable in the Microchip Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

The following equations give the relationship between thermal resistance, temperature gradient, and power.

#### EQUATION 1-1:

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

#### EQUATION 1-2:

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

#### EQUATION 1-3:

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

Where,

- $\theta_{JA}$  = Junction-to-air thermal resistance
- $\theta_{JB}$  = Junction-to-board thermal resistance
- $\theta_{JC}$  = Junction-to-case thermal resistance
- $T_J$  = Junction temperature
- $T_A$  = Ambient temperature
- $T_B$  = Board temperature (measured 1.0 mm away from the package edge)
- $T_C$  = Case temperature
- P = Total power dissipated by the device

The following table lists the package thermal resistance characteristics for M2GL.

**TABLE 1-7: PACKAGE THERMAL RESISTANCE**

| Product M2GL | $\theta_{JA}$ |         |         | $\theta_{JB}$ | $\theta_{JC}$ | Units |
|--------------|---------------|---------|---------|---------------|---------------|-------|
|              | Still Air     | 1.0 m/s | 2.5 m/s |               |               |       |
| <b>005</b>   |               |         |         |               |               |       |
| FGG484       | 19.36         | 15.81   | 14.63   | 9.74          | 5.27          | °C/W  |
| <b>010</b>   |               |         |         |               |               |       |
| FGG484       | 18.22         | 14.83   | 13.62   | 8.83          | 4.92          | °C/W  |
| <b>025</b>   |               |         |         |               |               |       |
| FGG484       | 17.03         | 13.66   | 12.45   | 7.66          | 4.18          | °C/W  |

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**TABLE 1-7: PACKAGE THERMAL RESISTANCE (CONTINUED)**

| Product M2GL | $\theta_{JA}$ |         |         | $\theta_{JB}$ | $\theta_{JC}$ | Units |
|--------------|---------------|---------|---------|---------------|---------------|-------|
|              | Still Air     | 1.0 m/s | 2.5 m/s |               |               |       |
| <b>060</b>   |               |         |         |               |               |       |
| FGG484       | 15.40         | 12.06   | 10.85   | 6.14          | 3.15          | °C/W  |
| <b>090</b>   |               |         |         |               |               |       |
| FGG484       | 14.64         | 11.37   | 10.16   | 5.43          | 2.77          | °C/W  |

### 1.3.2 THETA-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using [EQ 1-1](#).

#### EQUATION 1-1:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

The absolute maximum junction temperature is 135 °C. [EQ 1-3](#) shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL060TS-1FGG484 package at Automotive Grade 1 temperature and in still air, where:

#### EQUATION 1-2:

$$\begin{aligned}\theta_{JA} &= 15.4 \text{ °C/W} \text{ (taken from Table 1-7 on page 7).} \\ T_A &= 105 \text{ °C}\end{aligned}$$

#### EQUATION 1-3:

$$\text{Maximum Power Allowed} = \frac{135^\circ\text{C} - 105^\circ\text{C}}{15.4^\circ\text{C/W}} = 1.9 \text{ W}$$

The power consumption of a device can be calculated using the Microchip power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

### 1.3.3 THETA-JB

Junction-to-board thermal resistance ( $\theta_{JB}$ ) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### 1.3.4 THETA-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

## 1.4 Power Consumption

### 1.4.1 QUIESCENT SUPPLY CURRENT

The following table lists the quiescent supply current characteristics.

**TABLE 1-8: QUIESCENT SUPPLY CURRENT CHARACTERISTICS**

| Power Supplies/Blocks               | Modes and Configurations |                   | Notes |
|-------------------------------------|--------------------------|-------------------|-------|
|                                     | Non-Flash*Freeze Mode    | Flash*Freeze Mode |       |
| FPGA Core                           | On                       | Off               | —     |
| VDD                                 | On                       | On                | —     |
| VPP / VPPNVM                        | On                       | On                | —     |
| CCC_XX[01]_PLL_VDDA                 | 0 V                      | 0 V               | —     |
| VDDIx                               | On                       | On                | 1, 2  |
| VREFx                               | On                       | On                | —     |
| HPMS_CLK                            | 32 kHz                   | 32 kHz            | —     |
| RAM                                 | On                       | Sleep state       | —     |
| HPMS Controller                     | 50 MHz                   | 50 MHz            | —     |
| 50 MHz Oscillator (enable/disable)  | Enabled                  | Disabled          | —     |
| 1 MHz Oscillator (enable/disable)   | Disabled                 | Disabled          | —     |
| Crystal Oscillator (enable/disable) | Disabled                 | Disabled          | —     |

**Note 1:** VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, see the “Recommendation for Unused Bank Supplies” table in the [AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note](#).

**2:** No Differential (that is to say, LVDS) I/O’s or ODT attributes to be used.

The following table lists the quiescent supply current characteristics for the typical process.

**TABLE 1-9: IGLOO® 2 QUIESCENT SUPPLY CURRENT – TYPICAL PROCESS**

| Parameter | Modes            | Conditions                                       | 005        | 010        | 025        | 060        | 090        | Units |
|-----------|------------------|--|------------|------------|------------|------------|------------|-------|
|           |                  |  | VDD = 1.2V |       |
| IDC1      | Non-Flash*Freeze | Typical ( $T_J = 25^\circ\text{C}$ )             | 6.2        | 6.9        | 8.9        | 15.3       | 15.4       | mA    |
|           |                  | Automotive Grade 1 ( $T_J = 135^\circ\text{C}$ ) | 81.3       | 97.5       | 142.6      | 289.6      | 292.5      | mA    |
| IDC2      | Flash*Freeze     | Typical ( $T_J = 25^\circ\text{C}$ )             | 1.4        | 2.6        | 3.7        | 5.0        | 5.1        | mA    |
|           |                  | Automotive Grade 1 ( $T_J = 135^\circ\text{C}$ ) | 45.3       | 75.3       | 100.4      | 133.3      | 134.6      | mA    |

The following table lists the quiescent supply current characteristics for the worst-case process.

**TABLE 1-10: IGLOO® 2 QUIESCENT SUPPLY CURRENT – WORST-CASE PROCESS**

| Parameter | Modes            | Conditions                                       | 005         | 010         | 025         | 060         | 090         | Units |
|-----------|------------------|--|-------------|-------------|-------------|-------------|-------------|-------|
|           |                  |  | VDD = 1.26V |       |
| IDC1      | Non-Flash*Freeze | Automotive Grade 1 ( $T_J = 135^\circ\text{C}$ ) | 154.0       | 203.5       | 306.1       | 591.4       | 597.3       | mA    |

**TABLE 1-10: IGLOO® 2 QUIESCENT SUPPLY CURRENT – WORST-CASE PROCESS**

| Parameter | Modes         | Conditions                                       | 005         | 010         | 025         | 060         | 090         | Units |
|-----------|---------------|--|-------------|-------------|-------------|-------------|-------------|-------|
|           |               |  | VDD = 1.26V |       |
| IDC2      | Flash* Freeze | Automotive Grade 1 ( $T_J = 135^\circ\text{C}$ ) | 109.8       | 172.0       | 195.1       | 261.2       | 263.9       | mA    |

#### 1.4.2 PROGRAMMING CURRENTS

The following tables represent programming, verify, and Inrush currents for IGLOO 2 FPGA devices.

**TABLE 1-11: CURRENTS DURING PROGRAM CYCLE,  $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ , TYPICAL PROCESS**

| Power Supplies  | Voltage (V) | 005 | 010 | 025 | 060 | 090 | Units | Notes |
|-----------------|-------------|-----|-----|-----|-----|-----|-------|-------|
| VDD             | 1.26        | 46  | 53  | 55  | 30  | 42  | mA    | —     |
| VPP             | 3.46        | 8   | 11  | 6   | 9   | 12  | mA    | —     |
| VPPNVM          | 3.46        | 1   | 2   | 2   | 3   | 3   | mA    | *     |
| VDDI            | 2.62        | 31  | 16  | 17  | 12  | 12  | mA    | —     |
|                 | 3.46        | 62  | 31  | 36  | 12  | 17  | mA    | —     |
| Number of banks |             | 7   | 8   | 8   | 10  | 9   | —     | —     |

**Note:** \* VPP and VPPNVM are internally shorted.

**TABLE 1-12: CURRENTS DURING VERIFY CYCLE,  $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ , TYPICAL PROCESS**

| Power Supplies  | Voltage (V) | 005 | 010 | 025 | 060 | 090 | Units | Notes |
|-----------------|-------------|-----|-----|-----|-----|-----|-------|-------|
| VDD             | 1.26        | 44  | 53  | 55  | 33  | 41  | mA    | —     |
| VPP             | 3.46        | 6   | 5   | 3   | 8   | 11  | mA    | —     |
| VPPNVM          | 3.46        | 1   | 0   | 0   | 1   | 1   | mA    | —     |
| VDDI            | 2.62        | 31  | 16  | 17  | 12  | 11  | mA    | —     |
|                 | 3.46        | 61  | 32  | 36  | 12  | 17  | mA    | —     |
| Number of banks |             | 7   | 8   | 8   | 10  | 9   | —     | —     |

**TABLE 1-13: INRUSH CURRENTS AT POWER UP,  $-40^\circ\text{C} \leq T_J \leq 135^\circ\text{C}$ , TYPICAL PROCESS**

| Power Supplies  | Voltage (V) | 005 | 010 | 025 | 060 | 090 | Units |
|-----------------|-------------|-----|-----|-----|-----|-----|-------|
| VDD             | 1.26        | 36  | 53  | 78  | 45  | 98  | mA    |
| VPP             | 3.46        | 35  | 57  | 50  | 13  | 36  | mA    |
| VDDI            | 2.62        | 134 | 141 | 161 | 93  | 283 | mA    |
| Number of banks |             | 7   | 8   | 8   | 10  | 9   | —     |

#### 1.5 Average Fabric Temperature and Voltage Derating Factors

The following table lists the average temperature and voltage derating factors for fabric timing delay.

**TABLE 1-14: AVERAGE TEMPERATURE AND VOLTAGE DERATING FACTORS FOR FABRIC TIMING DELAYS—(NORMALIZED TO  $T_J = 135^\circ\text{C}$ , WORST-CASE VDD = 1.14V)**

| Array Voltage VDD (V) | Junction Temperature (°C) |        |      |       |       |       |        |        |        |
|-----------------------|---------------------------|--------|------|-------|-------|-------|--------|--------|--------|
|                       | -55 °C                    | -40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C | 125 °C | 135 °C |
| 1.14                  | 0.91                      | 0.91   | 0.93 | 0.93  | 0.95  | 0.96  | 0.97   | 1.00   | 1.00   |
| 1.2                   | 0.82                      | 0.82   | 0.84 | 0.84  | 0.86  | 0.87  | 0.88   | 0.90   | 0.90   |

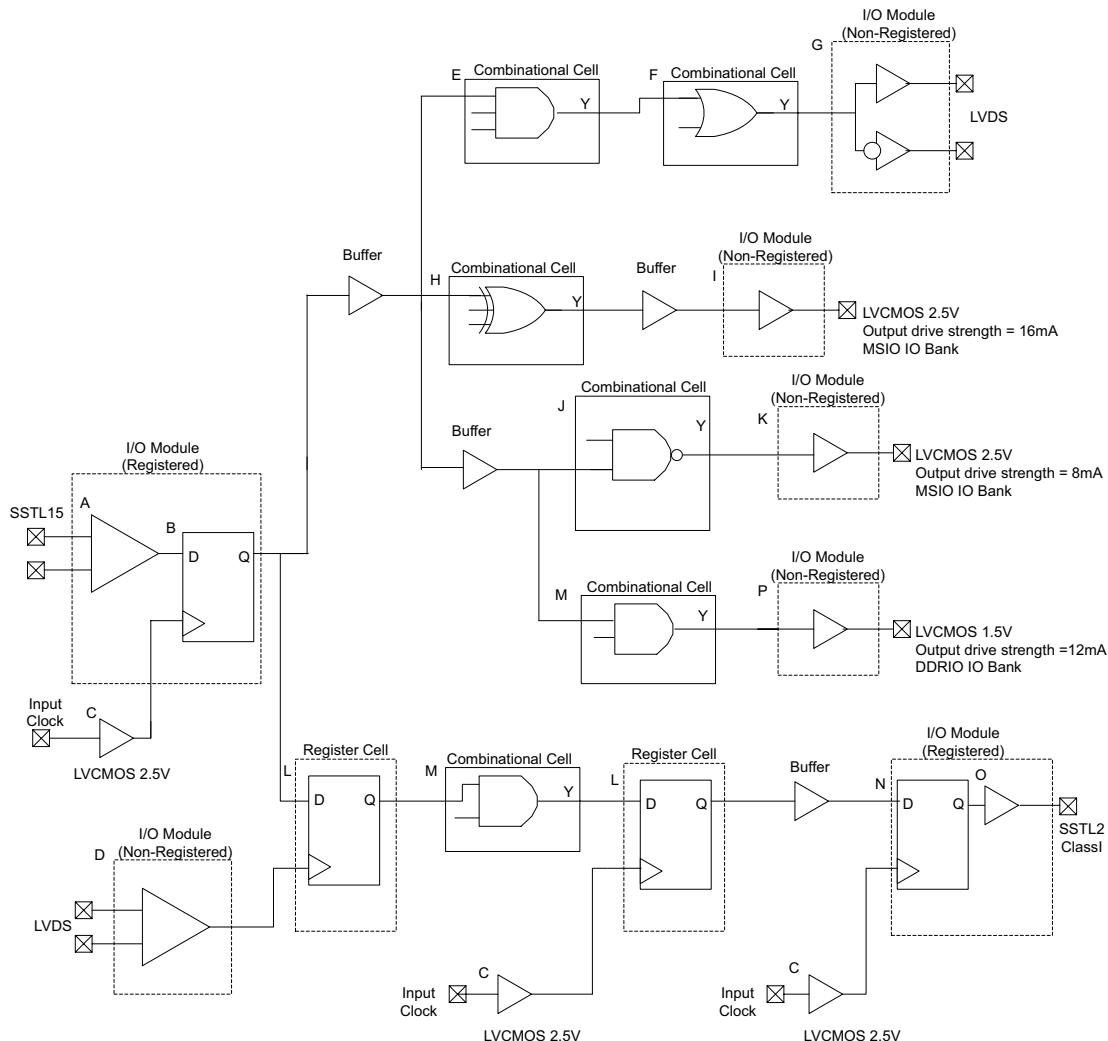
**TABLE 1-14: AVERAGE TEMPERATURE AND VOLTAGE DERATING FACTORS FOR FABRIC TIMING DELAYS—(NORMALIZED TO  $T_J = 135^\circ\text{C}$ , WORST-CASE VDD = 1.14V)**

|      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|
| 1.26 | 0.75 | 0.75 | 0.76 | 0.77 | 0.79 | 0.80 | 0.80 | 0.82 | 0.83 |
|------|------|------|------|------|------|------|------|------|------|

## 1.6 Timing Model

The following figure shows the timing delay.

**FIGURE 1-2: TIMING MODEL**



The following table lists the timing model parameters.

**TABLE 1-15: TIMING MODEL PARAMETERS**

| Index | Parameter | Description                          | Speed Grade -1 | Units | Notes  |
|-------|-----------|--------------------------------------|----------------|-------|--|
| A     | $t_{PY}$  | Propagation Delay of SSTL15 Receiver | 2.71           | ns    | For more information, see <a href="#">Table 2-55</a> |

**TABLE 1-15: TIMING MODEL PARAMETERS (CONTINUED)**

| Index | Parameter   | Description  | Speed Grade -1 | Units | Notes   |
|-------|-------------|--|----------------|-------|---|
| B     | $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register  | 0.166          | ns    | For more information, see <a href="#">Table 2-82</a>            |
|       | $t_{ISUD}$  | Setup Time of the Input Data Register  | 0.37           | ns    | For more information, see <a href="#">Table 2-82</a>            |
| C     | $t_{RCKH}$  | Input High Delay for Global Clock  | 1.915          | ns    | For more information, see <a href="#">Table 4-1 - Table 4-4</a> |
|       | $t_{RCKL}$  | Input Low Delay for Global Clock   | 1.08           | ns    | For more information, see <a href="#">Table 4-1 - Table 4-4</a> |
| D     | $t_{PY}$    | Input Propagation Delay of LVDS Receiver   | 3.085          | ns    | For more information, see <a href="#">Table 2-59</a>            |
| E     | $t_{DP}$    | Propagation Delay of a three input AND Gate  | 0.218          | ns    | For more information, see <a href="#">Table 3-1</a>             |
| F     | $t_{DP}$    | Propagation Delay of a OR Gate   | 0.17           | ns    | For more information, see <a href="#">Table 3-1</a>             |
| G     | $t_{DP}$    | Propagation Delay of a LVDS Transmitter  | 2.324          | ns    | For more information, see <a href="#">Table 2-60</a>            |
| H     | $t_{DP}$    | Propagation Delay of a three input XOR Gate  | 0.234          | ns    | For more information, see <a href="#">Table 3-1</a>             |
| I     | $t_{DP}$    | Propagation Delay of LVC MOS 2.5V Transmitter, Drive strength of 16mA on the MSIO Bank             | 2.746          | ns    | For more information, see <a href="#">Table 2-17</a>            |
| J     | $t_{DP}$    | Propagation Delay of a two input NAND Gate   | 0.17           | ns    | For more information, see <a href="#">Table 3-1</a>             |
| K     | $t_{DP}$    | Propagation Delay of LVC MOS 2.5V Transmitter, Drive strength of 8mA on the MSIO Bank              | 2.622          | ns    | For more information, see <a href="#">Table 2-17</a>            |
| L     | $t_{CLKQ}$  | Clock-to-Q of the Data Register  | 0.112          | ns    | For more information, see <a href="#">Table 2-82</a>            |
|       | $t_{SUD}$   | Setup Time of the Data Register  | 0.263          | ns    | For more information, see <a href="#">Table 2-82</a>            |
| M     | $t_{DP}$    | Propagation Delay of a two input AND gate  | 0.17           | ns    | For more information, see <a href="#">Table 3-1</a>             |
| N     | $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register   | 0.273          | ns    | For more information, see <a href="#">Table 2-83</a>            |
|       | $t_{OSUD}$  | Setup Time of the Output Data Register   | 0.197          | ns    | For more information, see <a href="#">Table 2-83</a>            |
| O     | $t_{DP}$    | Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank                                   | 2.308          | ns    | For more information, see <a href="#">Table 2-48</a>            |
| P     | $t_{DP}$    | Propagation Delay of LVC MOS 1.5V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank | 3.742          | ns    | For more information, see <a href="#">Table 2-30</a>            |

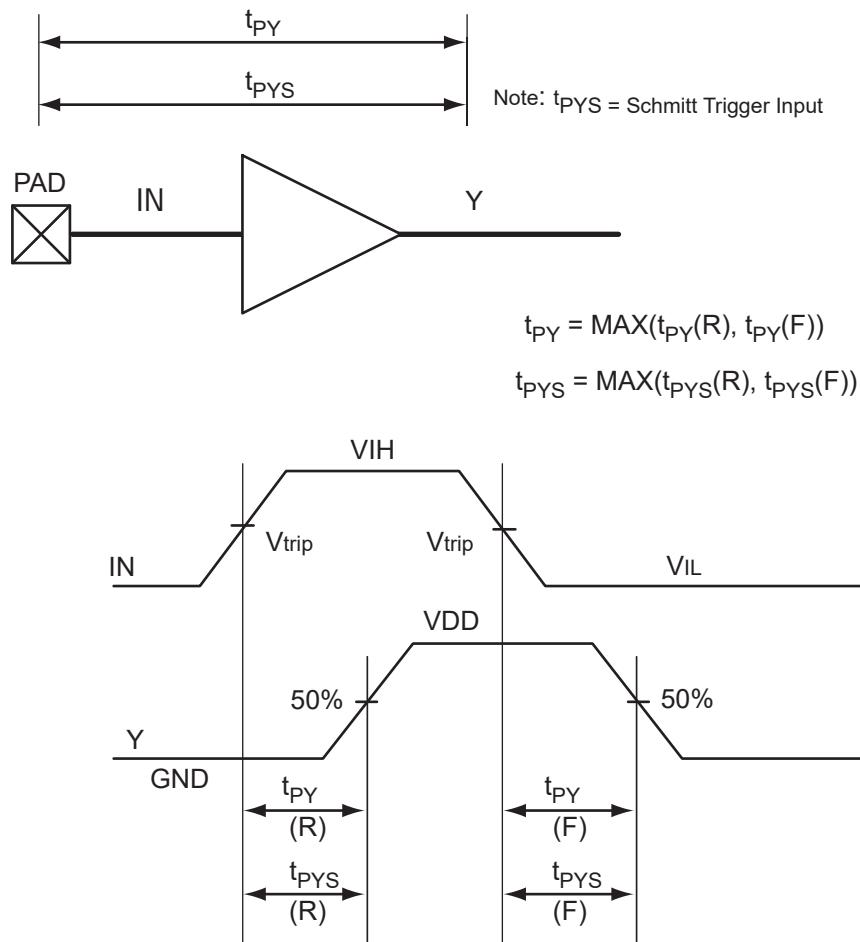
## 2.0 USER I/O CHARACTERISTICS

There are three types of I/Os supported in the IGLOO 2 FPGA family: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#). For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at: <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis>.

### 2.1 Input Buffer and AC Loading

The following figure shows the input buffer AC loading.

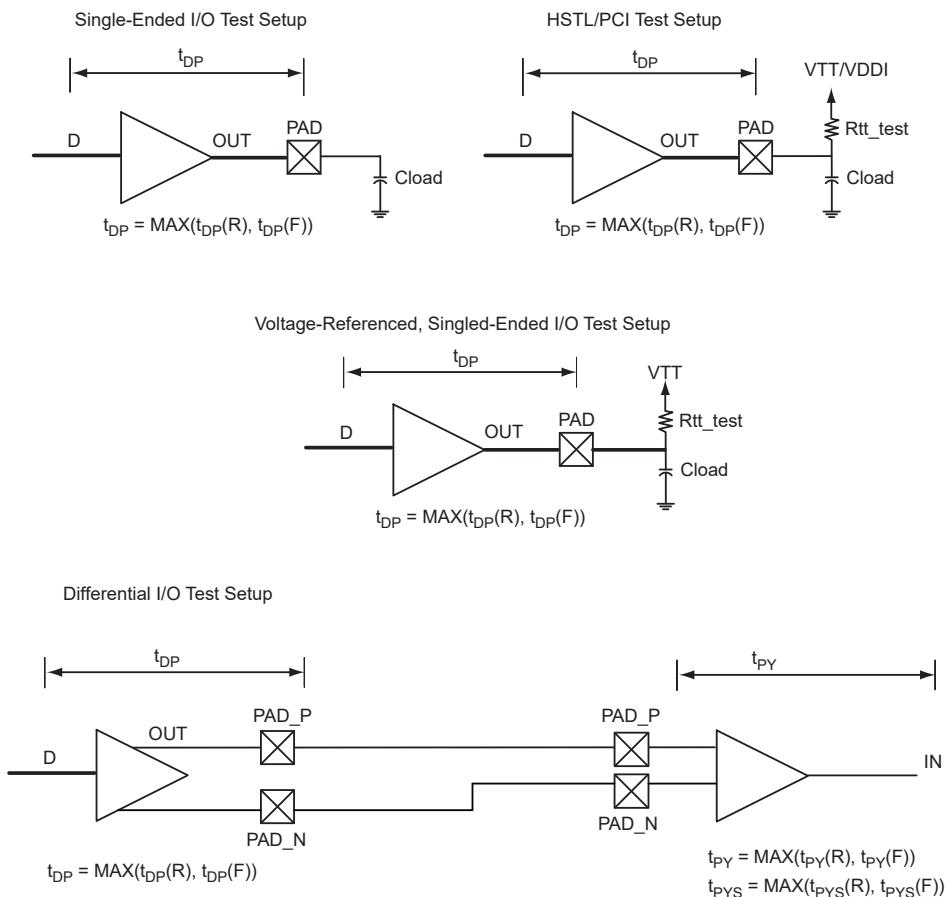
**FIGURE 2-1: INPUT BUFFER AC LOADING**



### 2.2 Output Buffer and AC Loading

The following figure shows the output buffer AC loading.

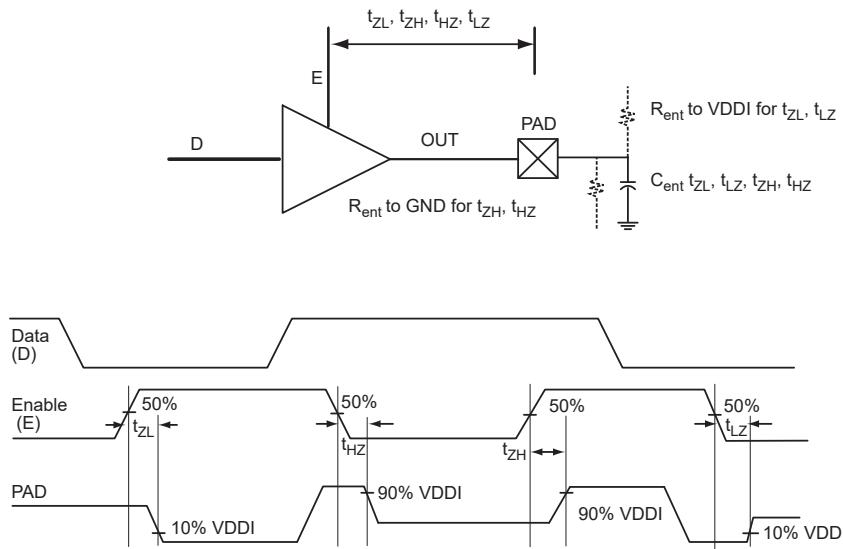
**FIGURE 2-2: OUTPUT BUFFER AC LOADING**



### 2.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point, as shown in the following figure. The following figure shows the tristate buffer for enable path test point.

**FIGURE 2-3: TRISTATE BUFFER FOR ENABLE PATH TEST POINT**



## 2.4 I/O Speeds

The following table lists the maximum data rate summary for the worst-case automotive grade 1 conditions.

**TABLE 2-1: MAXIMUM DATA RATE SUMMARY FOR WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS**

| Single-Ended I/O       | MSIO | MSIOD | DDRIO | Units |
|------------------------|------|-------|-------|-------|
| PCI 3.3V               | 560  | —     | —     | Mbps  |
| LVTTL 3.3V             | 540  | —     | —     | Mbps  |
| LVCMOS 3.3V            | 540  | —     | —     | Mbps  |
| LVCMOS 2.5V            | 360  | 370   | 360   | Mbps  |
| LVCMOS 1.8V            | 260  | 360   | 360   | Mbps  |
| LVCMOS 1.5V            | 140  | 190   | 210   | Mbps  |
| LVCMOS 1.2V            | 100  | 140   | 180   | Mbps  |
| Voltage-Referenced I/O | MSIO | MSIOD | DDRIO | Units |
| HSTL1.5V               | —    | —     | 360   | Mbps  |
| SSTL 2.5V              | 450  | 480   | 360   | Mbps  |
| SSTL 1.8V              | —    | —     | 600   | Mbps  |
| SSTL 1.5V              | —    | —     | 600   | Mbps  |
| Differential I/O       | MSIO | MSIOD | DDRIO | Units |
| LVPECL (input only)    | 810  | —     | —     | Mbps  |
| LVDS 3.3V              | 480  | 480   | —     | Mbps  |
| LVDS 2.5V              | 480  | 480   | —     | Mbps  |
| RSDS                   | 460  | 480   | —     | Mbps  |
| BLVDS                  | 450  | —     | —     | Mbps  |
| MLVDS                  | 450  | —     | —     | Mbps  |
| Mini-LVDS              | 460  | 480   | —     | Mbps  |

**TABLE 2-2: MAXIMUM FREQUENCY SUMMARY FOR WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS**

| Single-Ended I/O       | MSIO | MSIOD | DDRIO | Units |
|------------------------|------|-------|-------|-------|
| PCI 3.3V               | 280  | —     | —     | MHz   |
| LVTTL 3.3V             | 270  | —     | —     | MHz   |
| LVCMOS 3.3V            | 270  | —     | —     | MHz   |
| LVCMOS 2.5V            | 180  | 185   | 180   | MHz   |
| LVCMOS 1.8V            | 130  | 180   | 180   | MHz   |
| LVCMOS 1.5V            | 70   | 95    | 105   | MHz   |
| LVCMOS 1.2V            | 50   | 70    | 90    | MHz   |
| Voltage-Referenced I/O | MSIO | MSIOD | DDRIO | Units |
| HSTL 1.5V              | —    | —     | 180   | MHz   |
| SSTL 2.5V              | 225  | 240   | 180   | MHz   |
| SSTL 1.8V              | —    | —     | 300   | MHz   |
| SSTL 1.5V              | —    | —     | 300   | MHz   |
| Differential I/O       | MSIO | MSIOD | DDRIO | Units |
| LVPECL (input only)    | 405  | —     | —     | MHz   |
| LVDS 3.3V              | 240  | 240   | —     | MHz   |
| LVDS 2.5V              | 240  | 240   | —     | MHz   |
| RSDS                   | 230  | 240   | —     | MHz   |
| BLVDS                  | 225  | —     | —     | MHz   |
| MLVDS                  | 225  | —     | —     | MHz   |
| Mini-LVDS              | 230  | 240   | —     | MHz   |

## 2.5 Detailed I/O Characteristics

The following tables list the detailed I/O characteristics.

**TABLE 2-3: INPUT CAPACITANCE AND LEAKAGE CURRENT**

| Symbol                           | Definition   | Conditions               | Min | Max | Units |
|----------------------------------|--|--------------------------|-----|-----|-------|
| CIN                              | Input Capacitance  | —                        | —   | 10  | pF    |
| IIL (dc)                         | Input Current LOW<br>(Applicable to HSTL/SSTL inputs only)     | VDDI = 2.5V              | —   | 400 | uA    |
|                                  |  | VDDI = 1.8V              | —   | 500 | uA    |
|                                  |  | VDDI = 1.5V <sup>1</sup> | —   | 600 | uA    |
|                                  | Input Current LOW<br>(Applicable to all other digital inputs)  | —                        | —   | 10  | uA    |
| IIH (dc)                         | Input Current HIGH<br>(Applicable to HSTL/SSTL inputs only)    | VDDI = 2.5V              | —   | 400 | uA    |
|                                  |  | VDDI = 1.8V              | —   | 500 | uA    |
|                                  |  | VDDI = 1.5V <sup>1</sup> | —   | 600 | uA    |
|                                  | Input Current HIGH<br>(Applicable to all other digital inputs) | —                        | —   | 10  | uA    |
| T <sub>RAMPIN</sub> <sup>2</sup> | Input Ramp Time<br>(Applicable to all digital inputs)          | —                        | —   | 50  | ns    |

1. Applicable when IO pair is programmed with HSTL/SSTL IO type on IOP and an un-terminated IO type (LVCMOS, and so on) on ION pad.
2. Voltage ramp must be monotonic.

**TABLE 2-4: I/O WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES FOR DDRIO, MSIO, AND MSIOD BANKS—MINIMUM AND MAXIMUM WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES AT VOH/VOL LEVEL**

| VDDI Domain | DDRIO I/O Bank                           |        |  |        | MSIO I/O Bank                            |        |  |        | MSIOD I/O Bank                           |        |  |        | Notes |
|-------------|--|--------|--|--------|--|--------|--|--------|--|--------|--|--------|-------|
|             | $R_{(WEAK\ PULL-UP)}\ at\ VOH\ (\Omega)$ |        | $R_{(WEAK\ PULL-DOWN)}\ at\ VOL\ (\Omega)$ |        | $R_{(WEAK\ PULL-UP)}\ at\ VOH\ (\Omega)$ |        | $R_{(WEAK\ PULL-DOWN)}\ at\ VOL\ (\Omega)$ |        | $R_{(WEAK\ PULL-UP)}\ at\ VOH\ (\Omega)$ |        | $R_{(WEAK\ PULL-DOWN)}\ at\ VOL\ (\Omega)$ |        |       |
|             | Min                                      | Max    | Min  | Max    | Min                                      | Max    | Min  | Max    | Min                                      | Max    | Min  | Max    |       |
| 3.3V        | N/A                                      | N/A    | N/A  | N/A    | 9.9 K                                    | 17.1 K | 9.98 K                                     | 17.5 K | N/A                                      | N/A    | N/A  | N/A    | —     |
| 2.5V        | 10 K                                     | 17.8 K | 9.98 K                                     | 18 K   | 10 K                                     | 17.6 K | 10.1 K                                     | 18.4 K | 9.6 K                                    | 16.6 K | 9.5 K                                      | 16.4 K | 1, 2  |
| 1.8V        | 10.3 K                                   | 19.1 K | 10.3 K                                     | 19.5 K | 10.4 K                                   | 19.1 K | 10.4 K                                     | 20.4 K | 9.7 K                                    | 17.3 K | 9.7 K                                      | 17.1 K | 1, 2  |
| 1.5V        | 10.6 K                                   | 20.2 K | 10.6 K                                     | 21.1 K | 10.7 K                                   | 20.4 K | 10.8 K                                     | 22.2 K | 9.9 K                                    | 18 K   | 9.8 K                                      | 17.6 K | 1, 2  |
| 1.2V        | 11.1 K                                   | 22.7 K | 11.2 K                                     | 24.6 K | 11.3 K                                   | 23.2 K | 11.5 K                                     | 26.7 K | 10.3 K                                   | 19.6 K | 10 K                                       | 19.1 K | 1, 2  |

**Note 1:**  $R_{(WEAK\ PULL-DOWN)} = (VOL_{spec})/I_{(WEAK\ PULL-DOWN\ MAX)}$   
**2:**  $R_{(WEAK\ PULL-UP)} = (VDDI_{max} - VOH_{spec})/I_{(WEAK\ PULL-UP\ MIN)}$

**TABLE 2-5: SCHMITT TRIGGER INPUT HYSTERESIS—HYSTERESIS VOLTAGE VALUE FOR SCHMITT TRIGGER MODE INPUT BUFFERS**

| Input Buffer Configuration        | Hysteresis Value (Typical, unless otherwise noted) |
|-----------------------------------|--|
| 3.3V LVTTL / LVCmos / PCI / PCI-X | $0.05 \times VDDI$ (Worst-case)                    |
| 2.5V LVCmos                       | $0.05 \times VDDI$ (Worst-case)                    |
| 1.8V LVCmos                       | $0.1 \times VDDI$ (Worst-case)                     |
| 1.5V LVCmos                       | 60 mV  |
| 1.2V LVCmos                       | 20 mV  |

## 2.6 Single-Ended I/O Standards

### 2.6.1 LOW VOLTAGE COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (LVCmos)

LVCmos is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCmos standards supported in IGLOO 2 FPGAs are: LVCmos12, LVCmos15, LVCmos18, LVCmos25, and LVCmos33.

### 2.6.2 3.3V LVCmos/LVTTL

LVCmos 3.3V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3V applications.

#### 2.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

The following tables list the minimum and maximum AC/DC input and output levels specifications.

**TABLE 2-6: LVTTL/LVCmos 3.3V DC VOLTAGE SPECIFICATION (APPLICABLE TO MSIO I/O BANK ONLY)**

| Symbol   | Parameters          | Min  | Typ | Max  | Units | Notes |
|--|---------------------|------|-----|------|-------|-------|
| <b>LVTTL/LVCmos 3.3V Recommended DC Operating Conditions</b> |                     |      |     |      |       |       |
| VDDI   | Supply voltage      | 3.15 | 3.3 | 3.45 | V     | —     |
| <b>LVTTL/LVCmos 3.3V DC Input Voltage Specification</b>      |                     |      |     |      |       |       |
| VIH (DC)   | DC input logic High | 2.0  | —   | 3.45 | V     | —     |

**TABLE 2-6: LVTT/LVCMOS 3.3V DC VOLTAGE SPECIFICATION (APPLICABLE TO MSIO I/O BANK ONLY) (CONTINUED)**

|  |                      |                    |   |     |   |   |
|--|----------------------|--------------------|---|-----|---|---|
| VIL (DC)   | DC input logic Low   | -0.3               | — | 0.8 | V | — |
| IIH (DC)   | Input current High   | Refer to Table 2-3 | — | —   | — | — |
| IIL (DC)   | Input current Low    | Refer to Table 2-3 | — | —   | — | — |
| <b>LVC MOS 3.3V DC Output Voltage Specification</b>  |                      |                    |   |     |   |   |
| VOH  | DC output logic High | 2.4                | — | —   | V | * |
| VOL  | DC output logic Low  | —                  | — | 0.4 | V | * |
| <b>LVTT 3.3V DC Output Voltage Specification</b>   |                      |                    |   |     |   |   |
| VOH  | DC output logic High | 2.4                | — | —   | V | — |
| VOL  | DC output logic Low  | —                  | — | 0.4 | V | — |
| <b>Note:</b> * The VOH/VOL test points selected ensure compliance with LVC MOS 3.3 V JESD8-B requirements. |                      |                    |   |     |   |   |

**TABLE 2-7: LVTT/LVCMOS 3.3V MAXIMUM SWITCHING SPEEDS (APPLICABLE TO MSIO I/O BANK ONLY)**

| Symbol  | Parameters                               | Conditions                                 | Min | Typ | Max | Units |
|---|--|--|-----|-----|-----|-------|
| <b>LVTT/LVCMOS 3.3V Maximum Switching Speed</b> |  |  |     |     |     |       |
| Dmax  | Maximum data rate<br>(for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 540 | Mbps  |

**TABLE 2-8: LVTT/LVCMOS 3.3V AC TEST PARAMETER SPECIFICATIONS (APPLICABLE TO MSIO BANK ONLY)**

| LVTT/LVCMOS 3.3V AC Test Parameter Specifications |  |     |     |     |       |
|---|--|-----|-----|-----|-------|
| Symbol  | Parameters   | Min | Typ | Max | Units |
| Vtrip   | Measuring/trip point for data path   | —   | 1.4 | —   | V     |
| Rent  | Resistance for enable path<br>(t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> )         | —   | 2k  | —   | Ω     |
| Cent  | Capacitive loading for enable path<br>(t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> ) | —   | 5   | —   | pF    |
| Cload   | Capacitive loading for data path (t <sub>DP</sub> )  | —   | 5   | —   | pF    |

**TABLE 2-9: LVTT/LVCMOS 3.3V TRANSMITTER DRIVE STRENGTH SPECIFICATIONS (APPLICABLE TO MSIO BANK\* ONLY)**

| Output Drive Selection | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|---------|---------|-----------------|-----------------|
| 2 mA                   | 2.4     | 0.4     | 2               | 2               |
| 4 mA                   | 2.4     | 0.4     | 4               | 4               |
| 8 mA                   | 2.4     | 0.4     | 8               | 8               |
| 12 mA                  | 2.4     | 0.4     | 12              | 12              |
| 16 mA                  | 2.4     | 0.4     | 16              | 16              |
| 20 mA                  | 2.4     | 0.4     | 18              | 18              |

**Note:** \* Software Configurator GUI displays the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in Table 2-9.

### 2.6.2.2 AC Switching Characteristics

#### 2.6.2.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following tables list the AC switching characteristics for receiver (input buffers).

**TABLE 2-10: LVTT/LVCMOS 3.3V RECEIVER CHARACTERISTICS FOR MSIO I/O BANKS (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 3.15\text{ V}$**

|                                      | On-Die Termination<br>(ODT) in $\Omega$ | Speed Grade<br>-1 |           | Units |
|--------------------------------------|---|-------------------|-----------|-------|
|                                      |   | $t_{PY}$          | $t_{PYS}$ |       |
| LVTT/LVCMOS 3.3V (for MSIO I/O Bank) | None                                    | 2.435             | 2.463     | ns    |

#### 2.6.2.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**TABLE 2-11: LVTT/LVCMOS 3.3V TRANSMITTER CHARACTERISTICS FOR MSIO I/O BANK (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 3.15\text{ V}$**

| Output Drive Selection | Slew Control | Speed Grade<br>-1 |          |          |          |          | Units |
|------------------------|--------------|-------------------|----------|----------|----------|----------|-------|
|                        |              | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| 2 mA                   | slow         | 3.552             | 3.867    | 3.277    | 4.402    | 2.954    | ns    |
| 4 mA                   | slow         | 2.591             | 2.979    | 2.804    | 5.181    | 3.013    | ns    |
| 8 mA                   | slow         | 2.373             | 2.596    | 2.555    | 4.794    | 3.035    | ns    |
| 12 mA                  | slow         | 2.284             | 2.349    | 2.411    | 4.967    | 3.041    | ns    |
| 16 mA                  | slow         | 2.298             | 2.311    | 2.394    | 5.007    | 3.058    | ns    |
| 20 mA                  | slow         | 2.396             | 2.23     | 2.33     | 5.153    | 3.088    | ns    |

#### 2.6.3 2.5V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO 2 FPGAs in compliance to the JEDEC specification JESD8-5A.

##### 2.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

The following tables list the LVCMOS 2.5V DC voltage specification.

**TABLE 2-12: LVCMOS 2.5V DC VOLTAGE SPECIFICATION**

| Symbol   | Parameters   | Min                                | Typ | Max   | Units | Notes |
|--|--|------------------------------------|-----|-------|-------|-------|
| <b>LVCMOS 2.5V Recommended DC Operating Conditions</b> |  |                                    |     |       |       |       |
| VDDI   | Supply voltage                                     | 2.375                              | 2.5 | 2.625 | V     | —     |
| <b>LVCMOS 2.5V DC Input Voltage Specification</b>      |  |                                    |     |       |       |       |
| VIH (DC)   | DC input logic High (for MSIOD and DDRIO I/O Bank) | 1.7                                | —   | 2.625 | V     | —     |
| VIH (DC)   | DC input logic High (for MSIO I/O Bank)            | 1.7                                | —   | 2.75  | V     | —     |
| VIL (DC)   | DC input logic Low                                 | -0.3                               | —   | 0.7   | V     | —     |
| IIH (DC)   | Input current High                                 | Refer to <a href="#">Table 2-3</a> |     |       |       |       |
| IIL (DC)   | Input current Low                                  | Refer to <a href="#">Table 2-3</a> |     |       |       |       |
| <b>LVCMOS 2.5V DC Output Voltage Specification</b>     |  |                                    |     |       |       |       |
| VOH  | DC output logic High                               | 1.7                                | —   | —     | V     | *     |
| VOL  | DC output logic Low                                | —                                  | —   | 0.7   | V     | *     |

**Note:** \* The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

**TABLE 2-13: LVC MOS 2.5V MAXIMUM AC SWITCHING SPEEDS**

| Symbol | Parameters                                | Conditions                                      | Min | Typ | Max | Units |
|--------|---|---|-----|-----|-----|-------|
| Dmax   | Maximum data rate<br>(for DDRIO I/O Bank) | AC loading: 17 pF load,<br>maximum drive/slew   | —   | —   | 360 | Mbps  |
| Dmax   | Maximum data rate<br>(for MSIO I/O Bank)  | AC loading: 17 pF load, maxi-<br>mum drive/slew | —   | —   | 360 | Mbps  |
| Dmax   | Maximum data rate<br>(for MSIOD I/O Bank) | AC loading: 17 pF load, maxi-<br>mum drive/slew | —   | —   | 370 | Mbps  |

**TABLE 2-14: LVC MOS 2.5V AC TEST PARAMETERS AND DRIVER IMPEDANCE SPECIFICATIONS**

| Symbols   | Parameters   | Min | Typ                       | Max | Units |
|---|--|-----|---------------------------|-----|-------|
| <b>LVC MOS 2.5V Calibrated Impedance Option</b>       |  |     |                           |     |       |
| Rodt_cal  | Supported output driver calibrated<br>impedance (for DDRIO I/O Bank)   | —   | 75, 60, 50,<br>33, 25, 20 | —   | Ω     |
| <b>LVC MOS 2.5V AC Test Parameters Specifications</b> |  |     |                           |     |       |
| Vtrip   | Measuring/trip point for data path   | —   | 1.2                       | —   | V     |
| Rent  | Resistance for enable path<br>(t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> )         | —   | 2k                        | —   | Ω     |
| Cent  | Capacitive loading for enable path<br>(t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> ) | —   | 5                         | —   | pF    |
| Cload   | Capacitive loading for data path (t <sub>DP</sub> )  | —   | 5                         | —   | pF    |

**TABLE 2-15: LVC MOS 2.5V TRANSMITTER DRIVE STRENGTH SPECIFICATIONS**

| Output Drive Selection |                    |   | VOH (V)<br>Min | VOL (V)<br>Max | OH (at VOH)<br>mA | OL (at VOL)<br>mA |
|------------------------|--------------------|---|----------------|----------------|-------------------|-------------------|
| MSIO<br>I/O Bank       | MSIOD I/<br>O Bank | DDRIO I/O Bank<br>(With Software Default<br>Fixed Code) |                |                |                   |                   |
| 2 mA                   | 2 mA               | 2 mA  | VDDI - 0.4     | 0.7            | 2                 | 2                 |
| 4 mA                   | 4 mA               | 4 mA  | VDDI - 0.4     | 0.7            | 4                 | 4                 |
| 6 mA                   | 6 mA               | 6 mA  | VDDI - 0.4     | 0.7            | 6                 | 6                 |
| 8 mA                   | 8 mA               | 8 mA  | VDDI - 0.4     | 0.7            | 8                 | 8                 |
| 12 mA                  | 12 mA              | 12 mA   | VDDI - 0.4     | 0.7            | 12                | 12                |
| 16 mA                  | N/A                | 16 mA   | VDDI - 0.4     | 0.7            | 16                | 16                |

### 2.6.3.2 AC Switching Characteristics

#### 2.6.3.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following tables list the AC switching characteristics for receiver.

**TABLE 2-16: LVC MOS 2.5V AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT  
BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS: T<sub>J</sub> = 135 °C, VDD  
= 1.14V, VDDI = 2.375 V**

|                                   | On-Die Termination<br>(ODT) in Ω | Speed Grade<br>-1 |                  | Units |
|-----------------------------------|----------------------------------|-------------------|------------------|-------|
|                                   |                                  | t <sub>PY</sub>   | t <sub>PYS</sub> |       |
| LVC MOS 2.5V (for DDRIO I/O Bank) | None                             | 1.915             | 2.034            | ns    |
| LVC MOS 2.5V (for MSIO I/O Bank)  | None                             | 2.71              | 2.719            | ns    |
| LVC MOS 2.5V (for MSIOD I/O Bank) | None                             | 2.465             | 2.479            | ns    |

### 2.6.3.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following tables list the AC switching characteristics for transmitter (output and tristate buffers).

**TABLE 2-17: LVC MOS 2.5V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 2.375\text{V}$**

| Output Drive Selection                                    | Slew Control | Speed Grade -1 |          |          |          |          | Units |
|---|--------------|----------------|----------|----------|----------|----------|-------|
|   |              | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| <b>LVC MOS 2.5V (for DDRIO I/O Bank with Fixed Codes)</b> |              |                |          |          |          |          |       |
| 2 mA  | slow         | 4.009          | 3.703    | 4.028    | 3.441    | 3.005    | ns    |
|   | medium       | 3.664          | 3.416    | 3.686    | 2.98     | 2.545    | ns    |
|   | medium_fast  | 3.522          | 3.293    | 3.544    | 2.728    | 2.328    | ns    |
|   | fast         | 3.495          | 3.287    | 3.517    | 2.707    | 2.307    | ns    |
| 4 mA  | slow         | 3.407          | 2.973    | 3.398    | 3.536    | 3.184    | ns    |
|   | medium       | 3.096          | 2.73     | 3.091    | 3.055    | 2.645    | ns    |
|   | medium_fast  | 2.957          | 2.593    | 2.951    | 2.761    | 2.381    | ns    |
|   | fast         | 2.941          | 2.586    | 2.936    | 2.748    | 2.361    | ns    |
| 6 mA  | slow         | 3.223          | 2.744    | 3.202    | 3.664    | 3.279    | ns    |
|   | medium       | 2.917          | 2.499    | 2.906    | 3.13     | 2.689    | ns    |
|   | medium_fast  | 2.778          | 2.38     | 2.767    | 2.819    | 2.414    | ns    |
|   | fast         | 2.76           | 2.37     | 2.748    | 2.794    | 2.388    | ns    |
| 8 mA  | slow         | 3.166          | 2.674    | 3.142    | 3.709    | 3.332    | ns    |
|   | medium       | 2.862          | 2.432    | 2.85     | 3.159    | 2.715    | ns    |
|   | medium_fast  | 2.727          | 2.316    | 2.714    | 2.836    | 2.434    | ns    |
|   | fast         | 2.713          | 2.306    | 2.699    | 2.816    | 2.417    | ns    |
| 12 mA   | slow         | 3.045          | 2.53     | 3.016    | 3.7598   | 3.327    | ns    |
|   | medium       | 2.749          | 2.308    | 2.735    | 3.193    | 2.709    | ns    |
|   | medium_fast  | 2.62           | 2.198    | 2.605    | 2.848    | 2.436    | ns    |
|   | fast         | 2.608          | 2.189    | 2.593    | 2.823    | 2.42     | ns    |
| 16 mA   | slow         | 2.967          | 2.441    | 2.933    | 3.859    | 3.428    | ns    |
|   | medium       | 2.689          | 2.229    | 2.673    | 3.241    | 2.77     | ns    |
|   | medium_fast  | 2.563          | 2.125    | 2.546    | 2.896    | 2.48     | ns    |
|   | fast         | 2.55           | 2.115    | 2.532    | 2.869    | 2.457    | ns    |
| <b>LVC MOS 2.5V (for MSIO I/O Bank)</b>                   |              |                |          |          |          |          |       |
| 2 mA  | slow         | 3.975          | 4.398    | 4.265    | 5.147    | 3.257    | ns    |
| 4 mA  | slow         | 2.937          | 3.459    | 3.545    | 5.662    | 3.313    | ns    |
| 6 mA  | slow         | 2.716          | 3.027    | 3.188    | 5.714    | 3.342    | ns    |
| 8 mA  | slow         | 2.622          | 2.908    | 3.102    | 6.003    | 3.336    | ns    |
| 12 mA   | slow         | 2.651          | 2.761    | 2.975    | 5.978    | 3.34     | ns    |
| 16 mA   | slow         | 2.746          | 2.645    | 2.87     | 6.188    | 3.375    | ns    |
| <b>LVC MOS 2.5V (for MSIOD I/O Bank)</b>                  |              |                |          |          |          |          |       |
| 2 mA  | slow         | 2.428          | 2.953    | 2.921    | 2.5      | 2.401    | ns    |
| 4 mA  | slow         | 2.018          | 2.472    | 2.495    | 2.506    | 2.399    | ns    |
| 6 mA  | slow         | 1.88           | 2.354    | 2.401    | 2.551    | 2.437    | ns    |

**TABLE 2-17: LVC MOS 2.5V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $V_{DD} = 1.14\text{V}$ ,  $V_{DDI} = 2.375\text{V}$  (CONTINUED)**

| Output Drive Selection | Slew Control | Speed Grade -1 |          |          |          |          | Units |
|------------------------|--------------|----------------|----------|----------|----------|----------|-------|
|                        |              | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| 8 mA                   | slow         | 1.799          | 2.168    | 2.232    | 2.594    | 2.466    | ns    |
| 12 mA                  | slow         | 1.823          | 2.061    | 2.131    | 2.619    | 2.475    | ns    |

## 2.6.4 1.8V LVC MOS

LVC MOS 1.8 is a general standard for 1.8V applications and is supported in IGLOO 2 FPGAs in compliance to the JEDEC specification JESD8-7A.

### 2.6.4.1 Minimum and Maximum AC/DC Input and Output Levels

The following tables lists the 1.8V LVCC MOS minimum and maximum AC/DC input and output levels.

**TABLE 2-18: LVC MOS 1.8V DC VOLTAGE SPECIFICATION**

| Symbols   | Parameters  | Min                                | Typ | Max         | Units |
|---|---|------------------------------------|-----|-------------|-------|
| <b>Recommended DC Operating Conditions</b>          |   |                                    |     |             |       |
| VDDI  | Supply Voltage                                      | 1.710                              | 1.8 | 1.89        | V     |
| <b>LVC MOS 1.8V DC Input Voltage Specification</b>  |   |                                    |     |             |       |
| VIH(DC)   | DC input Logic HIGH (for MSIOD and DDRIO I/O Banks) | 0.65 x VDDI                        | —   | 1.89        | V     |
| VIH(DC)   | DC input Logic HIGH (for MSIO I/O Bank)             | 0.65 x VDDI                        | —   | 2.75        | V     |
| VIL(DC)   | DC input Logic LOW                                  | -0.3                               | —   | 0.35 x VDDI | V     |
| IIH(DC)   | Input Current HIGH                                  | Refer to <a href="#">Table 2-3</a> |     |             | —     |
| IIL(DC)   | Input Current LOW                                   | Refer to <a href="#">Table 2-3</a> |     |             | —     |
| <b>LVC MOS 1.8V DC Output Voltage Specification</b> |   |                                    |     |             |       |
| VOH   | DC output Logic HIGH                                | VDDI - 0.45                        | —   | —           | V     |
| VOL   | DC output Logic LOW                                 | —                                  | —   | 0.45        | V     |

**TABLE 2-19: LVC MOS 1.8V MAXIMUM AC SWITCHING SPEEDS**

| Symbols  | Parameters                             | Conditions                                 | Min | Typ | Max | Units |
|--|--|--|-----|-----|-----|-------|
| <b>LVC MOS 1.8V Maximum AC Switching Speed</b> |  |  |     |     |     |       |
| Dmax   | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 360 | Mbps  |
| Dmax   | Maximum data rate (for MSIO I/O Bank)  | AC loading: 17 pF load, maximum drive/slew | —   | —   | 260 | Mbps  |
| Dmax   | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 360 | Mbps  |

**Note:** \* Maximum data rate applies for drive strength 8mA and above, all slews

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**TABLE 2-20: LVCMS 1.8V TRANSMITTER DRIVE STRENGTH SPECIFICATIONS**

| Output Drive Selection |                | VOH (V)     | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|----------------|-------------|---------|-----------------|-----------------|
| MSIO I/O Bank          | MSIOD I/O Bank | Min         | Max     |                 |                 |
| 2 mA                   | 2 mA           | VDDI – 0.45 | 0.45    | 2               | 2               |
| 4 mA                   | 4 mA           | VDDI – 0.45 | 0.45    | 4               | 4               |
| 6 mA                   | 6 mA           | VDDI – 0.45 | 0.45    | 6               | 6               |
| 8 mA                   | 8 mA           | VDDI – 0.45 | 0.45    | 8               | 8               |
| 10 mA                  | 10 mA          | VDDI – 0.45 | 0.45    | 10              | 10              |
| 12 mA                  | N/A            | VDDI – 0.45 | 0.45    | 12              | 12              |

**TABLE 2-21: LVCMS 1.8V TRANSMITTER DRIVE STRENGTH SPECIFICATIONS**

| Output Drive Selection  | VOH (V)     | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA | Notes             |
|-------------------------|-------------|---------|-----------------|-----------------|-------------------|
|                         | Min         | Max     |                 |                 |                   |
| DDRIO Bank <sup>1</sup> |             |         |                 |                 |                   |
| 2 mA                    | VDDI – 0.45 | 0.45    | 2               | 2               | —                 |
| 4 mA                    | VDDI – 0.45 | 0.45    | 4               | 4               | —                 |
| 6 mA                    | VDDI – 0.45 | 0.45    | 6               | 6               | Note <sup>2</sup> |
| 8 mA                    | VDDI – 0.45 | 0.45    | 6               | 6               | Note <sup>2</sup> |
| 10 mA                   | VDDI – 0.45 | 0.45    | 8               | 8               | —                 |
| 12 mA                   | VDDI – 0.45 | 0.45    | 10              | 10              | —                 |
| 16 mA                   | VDDI – 0.45 | 0.45    | 12              | 12              | —                 |

**Note 1:** Software Configurator GUI will display the Commercial/Industrial numeric values. The actual drive capability at temperature is defined by [Table 2-21](#).

**2:** DDRIO has two 6mA drive strength settings. The setting that corresponds to Output Drive Selection value of 8mA has a shorter propagation delay.

**TABLE 2-22: LVCMS 1.8V AC TEST PARAMETERS AND DRIVER IMPEDANCE SPECIFICATIONS**

| LVCMS 1.8V AC Calibrated Impedance Option    |  |     |                        |     |       |
|--|--|-----|------------------------|-----|-------|
| Symbols                                      | Parameters   | Min | Typ                    | Max | Units |
| Rodt_cal                                     | Supported output driver calibrated impedance (for DDRIO I/O Bank)                | —   | 75, 60, 50, 33, 25, 20 | —   | Ω     |
| LVCMS 1.8V AC Test Parameters Specifications |  |     |                        |     |       |
| Vtrip  | Measuring/trip point for data path   | —   | 0.9                    | —   | V     |
| Rent   | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —   | 2k                     | —   | Ω     |
| Cent   | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —   | 5                      | —   | pF    |
| Cload  | Capacitive loading for data path ( $t_{DP}$ )                                    | —   | 5                      | —   | pF    |

#### 2.6.4.2 AC Switching Characteristics

##### 2.6.4.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-23: LVC MOS 1.8V AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $V_{DD} = 1.14\text{V}$ ,  $V_{DDI} = 1.7\text{ V}$**

|   | ODT<br>(On Die Termination) in $\Omega$ | Speed Grade<br>-1 |           | Units |
|---|---|-------------------|-----------|-------|
|   |   | $t_{PY}$          | $t_{PYS}$ |       |
| LVC MOS 1.8V<br>(for DDRIO I/O Bank with Fixed Codes) | None                                    | 2.085             | 2.228     | ns    |
| LVC MOS 1.8V (for MSIO I/O Bank)                      | None                                    | 3.212             | 3.197     | ns    |
|   | 50                                      | 3.423             | 3.425     | ns    |
|   | 75                                      | 3.35              | 3.343     | ns    |
|   | 150                                     | 3.279             | 3.266     | ns    |
| LVC MOS 1.8V (for MSIOD I/O Bank)                     | None                                    | 2.85              | 2.835     | ns    |
|   | 50                                      | 3.068             | 3.077     | ns    |
|   | 75                                      | 2.991             | 2.987     | ns    |
|   | 150                                     | 2.921             | 2.909     | ns    |

#### 2.6.4.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-24: LVCMS 1.8V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.71\text{V}$**

| Output Drive Selection                                  | Slew Control | Speed Grade -1 |          |          |          |          | Units |
|---|--------------|----------------|----------|----------|----------|----------|-------|
|   |              | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| <b>LVCMS 1.8V (for DDRIO I/O Bank with Fixed Codes)</b> |              |                |          |          |          |          |       |
| 2 mA  | slow         | 4.73           | 4.06     | 4.739    | 4.286    | 3.607    | ns    |
|   | medium       | 4.255          | 3.637    | 4.264    | 3.752    | 3.177    | ns    |
|   | medium_fast  | 4.02           | 3.428    | 4.028    | 3.413    | 2.896    | ns    |
|   | fast         | 3.994          | 3.409    | 4.003    | 3.385    | 2.874    | ns    |
| 4 mA  | slow         | 4.401          | 3.696    | 4.393    | 4.402    | 3.802    | ns    |
|   | medium       | 3.927          | 3.281    | 3.921    | 3.828    | 3.24     | ns    |
|   | medium_fast  | 3.694          | 3.082    | 3.686    | 3.468    | 2.93     | ns    |
|   | fast         | 3.673          | 3.065    | 3.665    | 3.441    | 2.908    | ns    |
| 6 mA  | slow         | 4.148          | 3.458    | 4.136    | 4.455    | 3.808    | ns    |
|   | medium       | 3.719          | 3.082    | 3.707    | 3.856    | 3.228    | ns    |
|   | medium_fast  | 3.513          | 2.898    | 3.5      | 3.484    | 2.934    | ns    |
|   | fast         | 3.487          | 2.879    | 3.474    | 3.45     | 2.909    | ns    |
| 8 mA  | slow         | 4.057          | 3.355    | 4.04     | 4.528    | 3.894    | ns    |
|   | medium       | 3.627          | 2.978    | 3.612    | 3.895    | 3.272    | ns    |
|   | medium_fast  | 3.419          | 2.79     | 3.402    | 3.506    | 2.957    | ns    |
|   | fast         | 3.392          | 2.775    | 3.376    | 3.476    | 2.932    | ns    |
| 10 mA   | slow         | 3.928          | 3.214    | 3.905    | 4.661    | 4.012    | ns    |
|   | medium       | 3.522          | 2.852    | 3.504    | 3.968    | 3.341    | ns    |
|   | medium_fast  | 3.315          | 2.67     | 3.295    | 3.545    | 2.997    | ns    |
|   | fast         | 3.292          | 2.655    | 3.272    | 3.521    | 2.967    | ns    |
| 12 mA   | slow         | 3.835          | 3.129    | 3.813    | 4.621    | 3.957    | ns    |
|   | medium       | 3.444          | 2.793    | 3.425    | 3.95     | 3.31     | ns    |
|   | medium_fast  | 3.249          | 2.626    | 3.228    | 3.536    | 2.98     | ns    |
|   | fast         | 3.229          | 2.611    | 3.208    | 3.505    | 2.959    | ns    |
| 16 mA   | slow         | 3.783          | 3.068    | 3.758    | 4.723    | 4.059    | ns    |
|   | medium       | 3.393          | 2.74     | 3.374    | 3.99     | 3.354    | ns    |
|   | medium_fast  | 3.209          | 2.573    | 3.186    | 3.567    | 3.007    | ns    |
|   | fast         | 3.189          | 2.558    | 3.166    | 3.531    | 2.986    | ns    |
| <b>LVCMS 1.8V (for MSIO I/O Bank)</b>                   |              |                |          |          |          |          |       |
| 2 mA  | slow         | 4              | 4.836    | 5.078    | 7.67     | 3.997    | ns    |
| 4 mA  | slow         | 3.707          | 4.207    | 4.534    | 7.71     | 4.018    | ns    |
| 6 mA  | slow         | 3.624          | 4.038    | 4.405    | 8.173    | 4.026    | ns    |
| 8 mA  | slow         | 3.654          | 3.823    | 4.207    | 8.251    | 4.03     | ns    |
| 10 mA   | slow         | 3.701          | 3.772    | 4.165    | 8.319    | 4.077    | ns    |
| 12 mA   | slow         | 3.79           | 3.654    | 4.05     | 8.413    | 4.156    | ns    |
| <b>LVCMS 1.8V (for MSIOD I/O Bank)</b>                  |              |                |          |          |          |          |       |

**TABLE 2-24: LVC MOS 1.8V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.71\text{V}$  (CONTINUED)**

| Output Drive Selection | Slew Control | Speed Grade -1 |          |          |          |          | Units |
|------------------------|--------------|----------------|----------|----------|----------|----------|-------|
|                        |              | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| 2 mA                   | slow         | 3.08           | 3.732    | 3.939    | 2.997    | 2.947    | ns    |
| 4 mA                   | slow         | 2.527          | 3.121    | 3.323    | 3.075    | 2.948    | ns    |
| 6 mA                   | slow         | 2.248          | 2.776    | 2.968    | 3.129    | 2.991    | ns    |
| 8 mA                   | slow         | 2.257          | 2.749    | 2.934    | 3.164    | 3.016    | ns    |
| 10 mA                  | slow         | 2.287          | 2.604    | 2.788    | 3.193    | 3.027    | ns    |

## 2.6.5 1.5V LVC MOS

LVC MOS 1.5 is a general standard for 1.5V applications and is supported in IGLOO 2 FPGAs in compliance to the JEDEC specification JESD8-11A.

### 2.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

The following tables list the minimum and maximum AC/DC input and output levels specification.

**TABLE 2-25: LVC MOS 1.5V MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| Symbols   | Parameters  | Min                                | Typ | Max                | Units |
|---|---|------------------------------------|-----|--------------------|-------|
| <b>LVC MOS 1.5V Recommended DC Operating Conditions</b> |   |                                    |     |                    |       |
| VDDI  | Supply voltage                                      | 1.425                              | 1.5 | 1.575              | V     |
| <b>LVC MOS 1.5V DC Input Voltage Specification</b>      |   |                                    |     |                    |       |
| VIH (DC)  | DC input logic High for (MSIOD and DDRIO I/O banks) | $0.65 \times VDDI$                 | —   | 1.575              | V     |
| VIH (DC)  | DC input logic High (for MSIO I/O Bank)             | $0.65 \times VDDI$                 | —   | 2.75               | V     |
| VIL (DC)  | DC input logic Low                                  | -0.3                               | —   | $0.35 \times VDDI$ | V     |
| IIH (DC)  | Input current High                                  | Refer to <a href="#">Table 2-3</a> |     |                    | —     |
| IIL (DC)  | Input current Low                                   | Refer to <a href="#">Table 2-3</a> |     |                    | —     |
| <b>LVC MOS 1.5V DC Output Voltage Specification</b>     |   |                                    |     |                    |       |
| VOH   | DC output logic High                                | $VDDI \times 0.75$                 | —   | —                  | V     |
| VOL   | DC output logic Low                                 | —                                  | —   | $VDDI \times 0.25$ | V     |

**TABLE 2-26: LVC MOS 1.5V MAXIMUM AC SWITCHING SPEEDS**

| Symbols  | Parameters                             | Conditions                                 | Min | Typ | Max | Units |
|--|--|--|-----|-----|-----|-------|
| <b>LVC MOS 1.5V Maximum AC Switching Speed</b> |  |  |     |     |     |       |
| Dmax   | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 210 | Mbps  |
| Dmax   | Maximum data rate (for MSIO I/O Bank)  | AC loading: 17 pF load, maximum drive/slew | —   | —   | 140 | Mbps  |
| Dmax   | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 190 | Mbps  |

**TABLE 2-27: LVC MOS 1.5V AC TEST PARAMETERS AND DRIVER IMPEDANCE SPECIFICATIONS**

| Symbols  | Parameters | Min | Typ | Max | Units |
|--|------------|-----|-----|-----|-------|
| <b>LVC MOS 1.5V AC Calibrated Impedance Option</b> |            |     |     |     |       |

**TABLE 2-27: LVC MOS 1.5V AC TEST PARAMETERS AND DRIVER IMPEDANCE SPECIFICATIONS (CONTINUED)**

| Symbols   | Parameters  | Min | Typ               | Max | Units |
|---|---|-----|-------------------|-----|-------|
| Rodt_cal  | Supported output driver calibrated impedance (for DDRIO I/O Bank)                   | —   | 75, 60, 50,<br>40 | —   | Ω     |
| <b>LVC MOS 1.5V AC Test Parameters Specifications</b> |   |     |                   |     |       |
| Vtrip   | Measuring/trip point for data path  | —   | 0.75              | —   | V     |
| Rent  | Resistance for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —   | 2k                | —   | Ω     |
| Cent  | Capacitive loading for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —   | 5                 | —   | pF    |
| Cload   | Capacitive loading for data path ( $t_{DP}$ )                                       | —   | 5                 | —   | pF    |

**TABLE 2-28: LVC MOS 1.5V TRANSMITTER DRIVE STRENGTH SPECIFICATIONS**

| Output Drive Selection |                |                                     | VOH (V)     | VOL (V)     | IOH (at VOH)<br>mA | IOL (at VOL)<br>mA |
|------------------------|----------------|-------------------------------------|-------------|-------------|--------------------|--------------------|
| MSIO I/O Bank          | MSIOD I/O Bank | DDRIO I/O Bank<br>(with Fixed Code) | Min         | Max         |                    |                    |
| 2 mA                   | 2 mA           | 2 mA                                | VDDI × 0.75 | VDDI × 0.25 | 2                  | 2                  |
| 4 mA                   | 4 mA           | 4 mA                                | VDDI × 0.75 | VDDI × 0.25 | 4                  | 4                  |
| 6 mA                   | 6 mA           | 6 mA                                | VDDI × 0.75 | VDDI × 0.25 | 6                  | 6                  |
| 8 mA                   | N/A            | 8 mA                                | VDDI × 0.75 | VDDI × 0.25 | 8                  | 8                  |
| N/A                    | N/A            | 10 mA                               | VDDI × 0.75 | VDDI × 0.25 | 10                 | 10                 |
| N/A                    | N/A            | 12 mA                               | VDDI × 0.75 | VDDI × 0.25 | 12                 | 12                 |

### 2.6.5.2 AC Switching Characteristics

#### 2.6.5.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-29: LVC MOS 1.5V AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $\text{VDD} = 1.14\text{V}$ ,  $\text{VDDI} = 1.425\text{V}$**

|   | ODT (On Die Termination)<br>in Ω | Speed Grade<br>-1 |           | Units |
|---|----------------------------------|-------------------|-----------|-------|
|   |                                  | $t_{PY}$          | $t_{PYS}$ |       |
| LVC MOS 1.5V (for DDRIO I/O Bank<br>with Fixed Codes) | None                             | 2.205             | 2.232     | ns    |
| LVC MOS 1.5V (for MSIO I/O Bank)                      | None                             | 3.711             | 3.684     | ns    |
|   | 50                               | 4.189             | 4.163     | ns    |
|   | 75                               | 4.019             | 3.988     | ns    |
|   | 150                              | 3.857             | 3.824     | ns    |
| LVC MOS 1.5V (for MSIOD I/O Bank)                     | None                             | 3.289             | 3.255     | ns    |
|   | 50                               | 3.792             | 3.771     | ns    |
|   | 75                               | 3.585             | 3.55      | ns    |
|   | 150                              | 3.423             | 3.387     | ns    |

#### 2.6.5.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-30: LVC MOS 1.5V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.425\text{V}$**

| Output Drive Selection                                    | Slew Control | Speed Grade -1 |          |          |          |          | Units |
|---|--------------|----------------|----------|----------|----------|----------|-------|
|   |              | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| <b>LVC MOS 1.5V (for DDRIO I/O Bank with Fixed Codes)</b> |              |                |          |          |          |          |       |
| 2 mA  | slow         | 5.774          | 4.847    | 5.796    | 4.791    | 4.916    | ns    |
|   | medium       | 5.149          | 4.32     | 5.168    | 4.382    | 3.638    | ns    |
|   | medium_fast  | 4.844          | 4.055    | 4.861    | 4.033    | 3.382    | ns    |
|   | fast         | 4.813          | 4.022    | 4.831    | 3.995    | 3.361    | ns    |
| 4 mA  | slow         | 5.019          | 4.177    | 5.008    | 4.998    | 4.184    | ns    |
|   | medium       | 4.459          | 3.658    | 4.447    | 4.457    | 3.764    | ns    |
|   | medium_fast  | 4.189          | 3.394    | 4.175    | 4.08     | 3.451    | ns    |
|   | fast         | 4.16           | 3.374    | 4.146    | 4.051    | 3.425    | ns    |
| 6 mA  | slow         | 4.795          | 3.911    | 4.778    | 5.201    | 4.416    | ns    |
|   | medium       | 4.257          | 3.418    | 4.239    | 4.56     | 3.831    | ns    |
|   | medium_fast  | 3.993          | 3.168    | 3.972    | 4.139    | 3.484    | ns    |
|   | fast         | 3.961          | 3.143    | 3.94     | 4.1      | 3.456    | ns    |
| 8 mA  | slow         | 4.652          | 3.73     | 4.633    | 5.247    | 4.461    | ns    |
|   | medium       | 4.125          | 3.276    | 4.105    | 4.575    | 3.826    | ns    |
|   | medium_fast  | 3.869          | 3.047    | 3.844    | 4.154    | 3.485    | ns    |
|   | fast         | 3.845          | 3.026    | 3.821    | 4.12     | 3.459    | ns    |
| 10 mA   | slow         | 4.568          | 3.65     | 4.547    | 5.352    | 4.559    | ns    |
|   | medium       | 4.069          | 3.211    | 4.047    | 4.645    | 3.876    | ns    |
|   | medium_fast  | 3.816          | 2.98     | 3.79     | 4.182    | 3.509    | ns    |
|   | fast         | 3.787          | 2.96     | 3.761    | 4.145    | 3.481    | ns    |
| 12 mA   | slow         | 4.504          | 3.6      | 4.48     | 5.389    | 4.644    | ns    |
|   | medium       | 4.007          | 3.163    | 3.985    | 4.657    | 3.917    | ns    |
|   | medium_fast  | 3.771          | 2.943    | 3.743    | 4.199    | 3.531    | ns    |
|   | fast         | 3.742          | 2.923    | 3.715    | 4.163    | 3.501    | ns    |
| <b>LVC MOS 1.5V (for MSIO I/O Bank)</b>                   |              |                |          |          |          |          |       |
| 2 mA  | slow         | 5.172          | 6.329    | 6.599    | 9.361    | 4.697    | ns    |
| 4 mA  | slow         | 4.707          | 5.233    | 5.71     | 10.259   | 4.757    | ns    |
| 6 mA  | slow         | 4.743          | 4.942    | 5.446    | 10.308   | 4.743    | ns    |
| 8 mA  | slow         | 4.928          | 4.712    | 5.237    | 10.738   | 4.811    | ns    |
| <b>LVC MOS 1.5V (for MSIOD I/O Bank)</b>                  |              |                |          |          |          |          |       |
| 2 mA  | slow         | 3.117          | 3.835    | 4.129    | 3.622    | 3.514    | ns    |
| 4 mA  | slow         | 2.76           | 3.401    | 3.67     | 3.718    | 3.557    | ns    |
| 6 mA  | slow         | 2.771          | 3.196    | 3.453    | 3.762    | 3.586    | ns    |

## 2.6.6 1.2V LVC MOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO 2 FPGAs in compliance to the JEDEC specification JESD8-12A.

#### 2.6.6.1 Minimum and Maximum Input and Output Levels Specification

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-31: LVCMOS 1.2V MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| Symbols  | Parameters  | Min                                | Typ | Max         | Units |
|--|---|------------------------------------|-----|-------------|-------|
| <b>LVCMOS 1.2V Recommended DC Operating Conditions</b> |   |                                    |     |             |       |
| VDDI<br>Supply voltage                                 |   | 1.140                              | 1.2 | 1.26        | V     |
| <b>LVCMOS 1.2V DC Input Voltage Specification</b>      |   |                                    |     |             |       |
| VIH (DC)   | DC input logic High (for MSIOD and DDRIO I/O Banks) | 0.65 × VDDI                        | —   | 1.26        | V     |
| VIH (DC)   | DC input logic High (for MSIO I/O Bank)             | 0.65 × VDDI                        | —   | 2.75        | V     |
| VIL (DC)   | DC input logic Low                                  | -0.3                               | —   | 0.35 × VDDI | V     |
| IIH (DC)   | Input current High                                  | Refer to <a href="#">Table 2-3</a> |     |             | —     |
| IIL (DC)   | Input current Low                                   | Refer to <a href="#">Table 2-3</a> |     |             | —     |
| <b>LVCMOS 1.2V DC Output Voltage Specification</b>     |   |                                    |     |             |       |
| VOH  | DC output logic High                                | VDDI × 0.75                        | —   | —           | V     |
| VOL  | DC output logic Low                                 | —                                  | —   | VDDI × 0.25 | V     |

**TABLE 2-32: LVCMOS 1.2V MAXIMUM AC SWITCHING SPEEDS**

| Symbols                                       | Parameters                             | Conditions                                 | Min | Typ | Max | Units |
|---|--|--|-----|-----|-----|-------|
| <b>LVCMOS 1.2V Maximum AC Switching Speed</b> |  |  |     |     |     |       |
| Dmax  | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 180 | Mbps  |
| Dmax  | Maximum data rate (for MSIO I/O Bank)  | AC loading: 17 pF load, maximum drive/slew | —   | —   | 100 | Mbps  |
| Dmax  | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | —   | —   | 140 | Mbps  |

**TABLE 2-33: LVCMOS 1.2V AC CALIBRATED IMPEDANCE AND TEST PARAMETERS SPECIFICATIONS**

| Symbols  | Parameters   | Min | Typ            | Max | Units |
|--|--|-----|----------------|-----|-------|
| <b>LVCMOS 1.2V AC Calibrated Impedance Option</b>    |  |     |                |     |       |
| Rodt_cal   | Supported output driver calibrated impedance (for DDRIO I/O Bank)                | —   | 75, 60, 50, 40 | —   | Ω     |
| <b>LVCMOS 1.2V AC Test Parameters Specifications</b> |  |     |                |     |       |
| Vtrip  | Measuring/trip point for data path   | —   | 0.6            | —   | V     |
| Rent   | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —   | 2k             | —   | Ω     |
| Cent   | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —   | 5              | —   | pF    |

**TABLE 2-33: LVC MOS 1.2V AC CALIBRATED IMPEDANCE AND TEST PARAMETERS SPECIFICATIONS (CONTINUED)**

| Symbols | Parameters                                    | Min | Typ | Max | Units |
|---------|---|-----|-----|-----|-------|
| Cload   | Capacitive loading for data path ( $t_{DP}$ ) | —   | 5   | —   | pF    |

**TABLE 2-34: LVC MOS 1.2V TRANSMITTER DRIVE STRENGTH SPECIFICATIONS**

| Output Drive Selection |                |                                     | VOH (V)     | VOL (V)     | IOH (at VOH)<br>mA | IOL (at VOL)<br>mA |
|------------------------|----------------|-------------------------------------|-------------|-------------|--------------------|--------------------|
| MSIO I/O Bank          | MSIOD I/O Bank | DDRIO I/O Bank<br>(with Fixed Code) | Min         | Max         |                    |                    |
| 2 mA                   | 2 mA           | 2 mA                                | VDDI × 0.75 | VDDI × 0.25 | 2                  | 2                  |
| 4 mA                   | 4 mA           | 4 mA                                | VDDI × 0.75 | VDDI × 0.25 | 4                  | 4                  |
| N/A                    | N/A            | 6 mA                                | VDDI × 0.75 | VDDI × 0.25 | 6                  | 6                  |

### 2.6.6.2 AC Switching Characteristics

#### 2.6.6.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-35: LVC MOS 1.2V AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.14\text{V}$**

|   | ODT (On Die Termination)<br>in $\Omega$ | Speed Grade<br>-1 |           | Units |
|---|---|-------------------|-----------|-------|
|   |   | $t_{PY}$          | $t_{PYS}$ |       |
| LVC MOS 1.2V (for DDRIO I/O Bank<br>with Fixed Codes) | None                                    | 2.557             | 2.574     | ns    |
| LVC MOS 1.2V (for MSIO I/O Bank)                      | None                                    | 4.932             | 4.889     | ns    |
|   | 50                                      | 6.746             | 6.667     | ns    |
|   | 75                                      | 5.978             | 5.901     | ns    |
|   | 150                                     | 5.339             | 5.283     | ns    |
| LVC MOS 1.2V (for MSIOD I/O Bank)                     | None                                    | 4.32              | 4.273     | ns    |
|   | 50                                      | 6.872             | 6.786     | ns    |
|   | 75                                      | 5.697             | 5.616     | ns    |
|   | 150                                     | 4.857             | 4.797     | ns    |

#### 2.6.6.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-36: LVC MOS 1.2V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.14\text{V}$**

| Output Drive<br>Selection                         | Slew Control | Speed Grade<br>-1 |          |          |          |          | Units |
|---|--------------|-------------------|----------|----------|----------|----------|-------|
|   |              | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| LVC MOS 1.2V (for DDRIO I/O Bank with Fixed Code) |              |                   |          |          |          |          |       |

**TABLE 2-36: LVCMS 1.2V AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.14\text{V}$  (CONTINUED)**

| Output Drive Selection                 | Slew Control | Speed Grade -1 |          |          |          |          | Units |
|--|--------------|----------------|----------|----------|----------|----------|-------|
|  |              | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| 2 mA                                   | slow         | 7.012          | 5.659    | 7.022    | 6.507    | 6.722    | ns    |
|  | medium       | 6.175          | 4.866    | 6.179    | 5.889    | 4.819    | ns    |
|  | medium_fast  | 5.736          | 4.456    | 5.737    | 5.383    | 4.462    | ns    |
|  | fast         | 5.693          | 4.426    | 5.694    | 5.348    | 4.431    | ns    |
| 4 mA                                   | slow         | 6.395          | 4.944    | 6.384    | 6.788    | 5.663    | ns    |
|  | medium       | 5.597          | 4.237    | 5.58     | 5.998    | 4.959    | ns    |
|  | medium_fast  | 5.173          | 3.873    | 5.152    | 5.456    | 4.534    | ns    |
|  | fast         | 5.126          | 3.846    | 5.105    | 5.414    | 4.499    | ns    |
| 6 mA                                   | slow         | 6.157          | 4.731    | 6.14     | 7.009    | 5.877    | ns    |
|  | medium       | 5.399          | 4.058    | 5.377    | 6.123    | 5.034    | ns    |
|  | medium_fast  | 5.002          | 3.699    | 4.974    | 5.508    | 4.574    | ns    |
|  | fast         | 4.955          | 3.661    | 4.928    | 5.449    | 4.533    | ns    |
| <b>LVCMS 1.2V (for MSIO I/O Bank)</b>  |              |                |          |          |          |          |       |
| 2 mA                                   | slow         | 7.126          | 7.94     | 8.633    | 13.977   | 6.504    | ns    |
| 4 mA                                   | slow         | 7.464          | 7.102    | 7.898    | 15.496   | 6.708    | ns    |
| <b>LVCMS 1.2V (for MSIOD I/O Bank)</b> |              |                |          |          |          |          |       |
| 2 mA                                   | slow         | 4.091          | 5.178    | 5.612    | 4.995    | 4.792    | ns    |
| 4 mA                                   | slow         | 3.982          | 4.453    | 4.866    | 5.064    | 4.859    | ns    |

## 2.6.7 3.3V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3V standards specify support for 33 MHz and 66 MHz PCI bus applications.

### 2.6.7.1 Minimum and Maximum Input and Output Levels Specification

The following table lists the minimum and maximum input and output levels specification.

**TABLE 2-37: PCI/PCI-X DC VOLTAGE SPECIFICATION (APPLICABLE TO MSIO BANK ONLY)**

| Symbols   | Parameters           | Min                                | Typ | Max  | Units |
|---|----------------------|------------------------------------|-----|------|-------|
| <b>PCI/PCIX Recommended DC Operating Conditions</b> |                      |                                    |     |      |       |
| VDDI  | Supply voltage       | 3.15                               | 3.3 | 3.45 | V     |
| <b>PCI/PCIX DC Input Voltage Specification</b>      |                      |                                    |     |      |       |
| VI  | DC input voltage     | 0                                  | —   | 3.45 | V     |
| IIH(DC)   | Input current High   | Refer to <a href="#">Table 2-3</a> |     |      | —     |
| IIL(DC)   | Input current Low    | Refer to <a href="#">Table 2-3</a> |     |      | —     |
| <b>PCI/PCIX DC Output Voltage Specification</b>     |                      |                                    |     |      |       |
| VOH   | DC output logic High | Per PCI Specification              |     |      | V     |
| VOL   | DC output logic Low  | Per PCI Specification              |     |      | V     |

---

**TABLE 2-38: PCI/PCI-X AC SPECIFICATIONS (APPLICABLE TO MSIO BANK ONLY)**

| Symbols  | Parameters   | Conditions                           | Min | Typ          | Max | Units |
|--|--|--------------------------------------|-----|--------------|-----|-------|
| <b>PCI/PCI-X AC Specifications</b>                 |  |                                      |     |              |     |       |
| Dmax   | Maximum data rate (MSIO I/O Bank)  | AC Loading: per JEDEC specifications | —   | —            | 560 | Mbps  |
| <b>PCI/PCI-X AC Test Parameters Specifications</b> |  |                                      |     |              |     |       |
| Vtrip  | Measuring/trip point for data path (falling edge)                                | —                                    | —   | 0.615 × VDDI | —   | V     |
| Vtrip  | Measuring/trip point for data path (rising edge)                                 | —                                    | —   | 0.285 × VDDI | —   | V     |
| Rtt_test   | Resistance for data test path  | —                                    | —   | 25           | —   | Ω     |
| Rent   | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —                                    | —   | 2k           | —   | Ω     |
| Cent   | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —                                    | —   | 5            | —   | pF    |
| Cload  | Capacitive loading for data path ( $t_{DP}$ )                                    | —                                    | —   | 10           | —   | pF    |

### 2.6.7.2 AC Switching Characteristics

#### 2.6.7.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-39: PCI/PCIX AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 3.15\text{V}$** 

|                                 | ODT<br>(On Die Termination)<br>in Ω | Speed Grade<br>-1 |           | Units |
|---------------------------------|-------------------------------------|-------------------|-----------|-------|
|                                 |                                     | $t_{PY}$          | $t_{PYS}$ |       |
| PCI/PCIX<br>(for MSIO I/O Bank) | None                                | 2.397             | 2.405     | ns    |

#### 2.6.7.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-40: PCI/PCIX AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 3.15\text{V}$** 

|                              | Speed Grade<br>-1 |          |          |          |          | Units |
|------------------------------|-------------------|----------|----------|----------|----------|-------|
|                              | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| PCI/PCIX (for MSIO I/O Bank) | 2.419             | 2.298    | 2.34     | 5.371    | 2.333    | ns    |

## 2.7 Voltage Referenced I/O Standards

### 2.7.1 HIGH-SPEED TRANSCEIVER LOGIC (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO 2 FPGA devices support two classes of the 1.5V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

### 2.7.1.1 Minimum and Maximum Input and Output Levels Specification

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-41: HSTL DC VOLTAGE SPECIFICATION (APPLICABLE TO DDRIO I/O BANK ONLY)**

| Symbols  | Parameters                       | Min                                | Typ   | Max        | Units |  |  |  |  |
|--|----------------------------------|------------------------------------|-------|------------|-------|--|--|--|--|
| <b>HSTL Recommended DC Operating Conditions</b>    |                                  |                                    |       |            |       |  |  |  |  |
| VDDI   | Supply voltage                   | 1.425                              | 1.5   | 1.575      | V     |  |  |  |  |
| VTT  | Termination voltage              | 0.698                              | 0.750 | 0.803      | V     |  |  |  |  |
| VREF   | Input reference voltage          | 0.698                              | 0.750 | 0.803      | V     |  |  |  |  |
| <b>HSTL DC Input Voltage Specification</b>         |                                  |                                    |       |            |       |  |  |  |  |
| VIH (DC)   | DC input logic High              | VREF + 0.1                         | —     | 1.575      | V     |  |  |  |  |
| VIL (DC)   | DC input logic Low               | -0.3                               | —     | VREF - 0.1 | V     |  |  |  |  |
| IIH (DC)   | Input current High               | Refer to <a href="#">Table 2-3</a> |       |            |       |  |  |  |  |
| IIL (DC)   | Input current Low                | Refer to <a href="#">Table 2-3</a> |       |            |       |  |  |  |  |
| <b>HSTL DC Output Voltage Specification</b>        |                                  |                                    |       |            |       |  |  |  |  |
| <b>HSTL Class I</b>                                |                                  |                                    |       |            |       |  |  |  |  |
| VOH  | DC output logic High             | VDDI - 0.4                         | —     | —          | V     |  |  |  |  |
| VOL  | DC output logic Low              | —                                  | —     | 0.4        | V     |  |  |  |  |
| IOH at VOH   | Output minimum source DC current | -7.0                               | —     | —          | mA    |  |  |  |  |
| IOL at VOL   | Output minimum sink current      | 7.0                                | —     | —          | mA    |  |  |  |  |
| <b>HSTL Class II</b>                               |                                  |                                    |       |            |       |  |  |  |  |
| VOH  | DC output logic High             | VDDI - 0.4                         | —     | —          | V     |  |  |  |  |
| VOL  | DC output logic Low              | —                                  | —     | 0.4        | V     |  |  |  |  |
| IOH at VOH   | Output minimum source DC current | -15.0                              | —     | —          | mA    |  |  |  |  |
| IOL at VOL   | Output minimum sink current      | 15.0                               | —     | —          | mA    |  |  |  |  |
| <b>HSTL DC Differential Voltage Specifications</b> |                                  |                                    |       |            |       |  |  |  |  |
| VID (DC)   | DC input differential voltage    | 0.2                                | —     | —          | V     |  |  |  |  |

**TABLE 2-42: HSTL AC SPECIFICATIONS (APPLICABLE TO DDRIO BANK ONLY)**

| Symbols  | Parameters  | Conditions                           | Min  | Typ           | Max | Units |
|--|---|--------------------------------------|------|---------------|-----|-------|
| <b>HSTL AC Differential Voltage Specifications</b> |   |                                      |      |               |     |       |
| VDIFF  | AC input differential voltage                                     | —                                    | 0.4  | —             | —   | V     |
| Vx   | AC differential cross point voltage                               | —                                    | 0.68 | —             | 0.9 | V     |
| <b>HSTL Maximum AC Switching Speed</b>             |   |                                      |      |               |     |       |
| Dmax   | Maximum data rate   | AC loading: per JEDEC specifications | —    | —             | 360 | Mbps  |
| <b>HSTL Impedance Specification</b>                |   |                                      |      |               |     |       |
| Rref   | Supported output driver calibrated impedance (for DDRIO I/O Bank) | Reference resistance = 191Ω          | —    | 25.5,<br>47.8 | —   | Ω     |
| RTT  | Effective impedance value (ODT for DDRIO I/O Bank only)           | Reference resistance = 191Ω          | —    | 47.8          | —   | Ω     |
| <b>HSTL AC Test Parameters Specification</b>       |   |                                      |      |               |     |       |

**TABLE 2-42: HSTL AC SPECIFICATIONS (APPLICABLE TO DDRIO BANK ONLY) (CONTINUED)**

| Symbols  | Parameters  | Conditions | Min | Typ  | Max | Units    |
|----------|---|------------|-----|------|-----|----------|
| Vtrip    | Measuring/trip point for data path  | —          | —   | 0.75 | —   | V        |
| Rent     | Resistance for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —          | —   | 2k   | —   | $\Omega$ |
| Cent     | Capacitive loading for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —          | —   | 5    | —   | pF       |
| Rtt_test | Reference resistance for data test path for HSTL15 Class I ( $t_{DP}$ )             | —          | —   | 50   | —   | $\Omega$ |
| Rtt_test | Reference resistance for data test path for HSTL15 Class II ( $t_{DP}$ )            | —          | —   | 25   | —   | $\Omega$ |
| Cload    | Capacitive loading for data path<br>( $t_{DP}$ )                                    | —          | —   | 5    | —   | pF       |

### 2.7.1.2 AC Switching Characteristics

#### 2.7.1.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-43: HSTL15 AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.425\text{V}$** 

| ODT (On Die Termination)<br>in $\Omega$          | $t_{PY}$          |       | Units |
|--|-------------------|-------|-------|
|  | Speed Grade<br>-1 |       |       |
| <b>HSTL (for DDRIO I/O Bank with Fixed Code)</b> |                   |       |       |
| Pseudo-Differential                              | None              | 1.683 | ns    |
| True-Differential                                | None              | 1.703 | ns    |

#### 2.7.1.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-44: HSTL 15 AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.425\text{V}$** 

|   | Speed Grade<br>-1 |          |          |          |          | Units |
|---|-------------------|----------|----------|----------|----------|-------|
|   | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| <b>HSTL Class I (for DDRIO I/O Bank)</b>  |                   |          |          |          |          |       |
| Single Ended                              | 2.953             | 2.941    | 2.935    | 3.375    | 2.808    | ns    |
| Differential                              | 2.937             | 2.786    | 2.785    | 5.796    | 4.844    | ns    |
| <b>HSTL Class II (for DDRIO I/O Bank)</b> |                   |          |          |          |          |       |
| Single Ended                              | 2.847             | 2.764    | 2.764    | 4.628    | 4.128    | ns    |
| Differential                              | 2.857             | 2.84     | 2.833    | 3.402    | 2.826    | ns    |

### 2.7.2 STUB-SERIES TERMINATED LOGIC

Stub-Series Terminated Logic (SSTL) for 2.5V (SSTL2), 1.8V (SSTL18), and 1.5V (SSTL15) is supported in IGLOO 2 FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15.

### 2.7.3 STUB-SERIES TERMINATED LOGIC 2.5V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO 2 FPGAs. IGLOO 2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### 2.7.3.1 Minimum and Maximum DC Input and Output Levels Specification

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-45: SSTL2 MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS**

| Symbols  | Parameters                       | Min                                | Typ   | Max         | Units |  |  |  |  |
|--|----------------------------------|------------------------------------|-------|-------------|-------|--|--|--|--|
| <b>Recommended DC Operating Conditions</b>                       |                                  |                                    |       |             |       |  |  |  |  |
| VDDI   | Supply voltage                   | 2.375                              | 2.5   | 2.625       | V     |  |  |  |  |
| VTT  | Termination voltage              | 1.164                              | 1.250 | 1.339       | V     |  |  |  |  |
| VREF   | Input reference voltage          | 1.164                              | 1.250 | 1.339       | V     |  |  |  |  |
| <b>SSTL2 DC Input Voltage Specification</b>                      |                                  |                                    |       |             |       |  |  |  |  |
| VIH (DC)   | DC input logic High              | VREF + 0.15                        | —     | 2.625       | V     |  |  |  |  |
| VIL (DC)   | DC input logic Low               | -0.3                               | —     | VREF - 0.15 | V     |  |  |  |  |
| IIH (DC)   | Input current High               | Refer to <a href="#">Table 2-3</a> |       |             |       |  |  |  |  |
| IIL (DC)   | Input current Low                | Refer to <a href="#">Table 2-3</a> |       |             |       |  |  |  |  |
| <b>SSTL2 DC Output Voltage Specification</b>                     |                                  |                                    |       |             |       |  |  |  |  |
| <b>SSTL2 Class I</b>   |                                  |                                    |       |             |       |  |  |  |  |
| VOH  | DC output logic High             | VTT + 0.608                        | —     | —           | V     |  |  |  |  |
| VOL  | DC output logic Low              | —                                  | —     | VTT - 0.608 | V     |  |  |  |  |
| IOH at VOH   | Output minimum source DC current | 8.1                                | —     | —           | mA    |  |  |  |  |
| IOL at VOL   | Output minimum sink current      | -8.1                               | —     | —           | mA    |  |  |  |  |
| <b>SSTL2 Class – Applicable to MSIO and DDRIO I/O Banks Only</b> |                                  |                                    |       |             |       |  |  |  |  |
| VOH  | DC output logic High             | VTT + 0.81                         | —     | —           | V     |  |  |  |  |
| VOL  | DC output logic Low              | —                                  | —     | VTT - 0.81  | V     |  |  |  |  |
| IOH at VOH   | Output minimum source DC current | 16.2                               | —     | —           | mA    |  |  |  |  |
| IOL at VOL   | Output minimum sink current      | -16.2                              | —     | —           | mA    |  |  |  |  |
| <b>SSTL2 DC Differential Voltage Specification</b>               |                                  |                                    |       |             |       |  |  |  |  |
| VID (DC)   | DC input differential voltage    | 0.3                                | —     | —           | V     |  |  |  |  |

**TABLE 2-46: SSTL2 AC SPECIFICATIONS**

| Symbols   | Parameters                             | Conditions                           | Min | Typ | Max | Units |
|---|--|--------------------------------------|-----|-----|-----|-------|
| <b>SSTL2 Maximum AC Switching Speeds</b>            |  |                                      |     |     |     |       |
| Dmax  | Maximum data rate (for DDRIO I/O Bank) | AC loading: per JEDEC specifications | —   | —   | 360 | Mbps  |
| Dmax  | Maximum data rate (for MSIO I/O Bank)  | AC loading: 17pF load                | —   | —   | 450 | Mbps  |
| Dmax  | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17pF load                | —   | —   | 480 | Mbps  |
| <b>SSTL2 AC Differential Voltage Specifications</b> |  |                                      |     |     |     |       |
| VDIFF   | AC Input Differential Voltage          | —                                    | 0.7 | —   | —   | V     |

**TABLE 2-46: SSTL2 AC SPECIFICATIONS (CONTINUED)**

| Symbols  | Parameters   | Conditions                | Min              | Typ    | Max              | Units |
|--|--|---------------------------|------------------|--------|------------------|-------|
| Vx   | AC Differential Cross Point Voltage  | —                         | 0.5 × VDDI - 0.2 | —      | 0.5 × VDDI + 0.2 | V     |
| <b>SSTL2 Impedance Specifications</b>          |  |                           |                  |        |                  |       |
|  | Supported output driver calibrated impedance (for DDRIO I/O Bank)                | Reference resistor = 150Ω | —                | 20, 42 | —                | Ω     |
| <b>SSTL2 AC Test Parameters Specifications</b> |  |                           |                  |        |                  |       |
| Vtrip  | Measuring/trip point for data path   | —                         | —                | 1.25   | —                | V     |
| Rent   | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —                         | —                | 2k     | —                | Ω     |
| Cent   | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —                         | —                | 5      | —                | pF    |
| Rtt_test                                       | Reference resistance for data test path for SSTL2 Class I ( $t_{DP}$ )           | —                         | —                | 50     | —                | Ω     |
| Rtt_test                                       | Reference resistance for data test path for SSTL2 Class II ( $t_{DP}$ )          | —                         | —                | 25     | —                | Ω     |
| Cload  | Capacitive loading for data path ( $t_{DP}$ )                                    | —                         | —                | 5      | —                | pF    |

### 2.7.3.2 AC Switching Characteristics

#### 2.7.3.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

The following tables list the AC switching characteristics for receiver.

**TABLE 2-47: SSTL2 AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 2.375\text{V}$**

|                               | ODT (On Die Termination) in Ω | Speed Grade<br>-1 | Units |
|-------------------------------|-------------------------------|-------------------|-------|
|                               |                               | $t_{PY}$          |       |
| <b>SSTL2 (DDRIO I/O Bank)</b> |                               |                   |       |
| Pseudo-Differential           | None                          | 1.621             | ns    |
| True-Differential             | None                          | 1.656             | ns    |
| <b>SSTL2 (MSIO I/O Bank)</b>  |                               |                   |       |
| Pseudo-Differential           | None                          | 3.106             | ns    |
| True-Differential             | None                          | 3.053             | ns    |
| <b>SSTL2 (MSIOD I/O Bank)</b> |                               |                   |       |
| Pseudo-Differential           | None                          | 2.742             | ns    |
| True-Differential             | None                          | 2.73              | ns    |

**TABLE 2-48: SSTL2 AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $V_{DD} = 1.14\text{V}$ ,  $V_{DDI} = 2.375\text{V}$**

|                       | Speed Grade<br>-1 |          |          |          |          | Units |  |
|-----------------------|-------------------|----------|----------|----------|----------|-------|--|
|                       | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |  |
| <b>SSTL2 Class I</b>  |                   |          |          |          |          |       |  |
| <b>DDRIO I/O Bank</b> |                   |          |          |          |          |       |  |
| Single Ended          | 2.484             | 2.169    | 2.16     | 4.995    | 4.827    | ns    |  |
| Differential          | 2.48              | 2.406    | 2.401    | 3.004    | 3.017    | ns    |  |
| <b>MSIO I/O Bank</b>  |                   |          |          |          |          |       |  |
| Single Ended          | 2.308             | 2.279    | 2.267    | 2.648    | 2.552    | ns    |  |
| Differential          | 2.46              | 2.731    | 2.72     | 2.64     | 2.546    | ns    |  |
| <b>MSIOD I/O Bank</b> |                   |          |          |          |          |       |  |
| Single Ended          | 1.663             | 1.608    | 1.606    | 2.462    | 2.286    | ns    |  |
| Differential          | 1.792             | 1.951    | 1.946    | 2.455    | 2.277    | ns    |  |
| <b>SSTL2 Class II</b> |                   |          |          |          |          |       |  |
| <b>DDRIO I/O Bank</b> |                   |          |          |          |          |       |  |
| Single Ended          | 2.343             | 2.082    | 2.076    | 4.286    | 4.14     | ns    |  |
| Differential          | 2.344             | 2.237    | 2.234    | 3.225    | 3.052    | ns    |  |
| <b>MSIO I/O Bank</b>  |                   |          |          |          |          |       |  |
| Single Ended          | 2.591             | 2.232    | 2.213    | 2.676    | 2.567    | ns    |  |
| Differential          | 2.732             | 2.593    | 2.582    | 2.663    | 2.566    | ns    |  |

## 2.7.4 STUB-SERIES TERMINATED LOGIC 1.8V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO 2 FPGAs. IGLOO 2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### 2.7.4.1 Minimum and Maximum Input and Output Levels Specification

The following table lists the minimum and maximum input and output levels specification.

**TABLE 2-49: SSTL18 AC/DC MINIMUM AND MAXIMUM INPUT AND OUTPUT LEVELS SPECIFICATION**

| Symbols                                      | Parameters              | Min                                | Typ   | Max          | Units | Notes |
|--|-------------------------|------------------------------------|-------|--------------|-------|-------|
| <b>Recommended DC Operating Conditions</b>   |                         |                                    |       |              |       |       |
| VDDI   | Supply voltage          | 1.71                               | 1.8   | 1.89         | V     | —     |
| VTT  | Termination voltage     | 0.838                              | 0.900 | 0.964        | V     | —     |
| VREF   | Input reference voltage | 0.838                              | 0.900 | 0.964        | V     | —     |
| <b>SSTL18 DC Input Voltage Specification</b> |                         |                                    |       |              |       |       |
| VIH (DC)                                     | DC input logic High     | VREF + 0.125                       | —     | 1.89         | V     | —     |
| VIL (DC)                                     | DC input logic Low      | -0.3                               | —     | VREF - 0.125 | V     | —     |
| IIH (DC)                                     | Input current High      | Refer to <a href="#">Table 2-3</a> |       |              | —     | —     |
| IIL (DC)                                     | Input current Low       | Refer to <a href="#">Table 2-3</a> |       |              | —     | —     |

**TABLE 2-49: SSTL18 AC/DC MINIMUM AND MAXIMUM INPUT AND OUTPUT LEVELS SPECIFICATION (CONTINUED)**

| Symbols   | Parameters   | Min         | Typ | Max         | Units | Notes |
|---|--|-------------|-----|-------------|-------|-------|
| <b>SSTL18 DC Output Voltage Specification</b>       |  |             |     |             |       |       |
| <b>SSTL18 Class I</b>                               |  |             |     |             |       |       |
| VOH   | DC output logic High                                   | VTT + 0.603 | —   | —           | V     | —     |
| VOL   | DC output logic Low                                    | —           | —   | VTT – 0.603 | V     | —     |
| IOH at VOH  | Output minimum source DC current (DDRIO I/O Bank only) | 6.0         | —   | —           | mA    | —     |
| IOL at VOL  | Output minimum sink current (DDRIO I/O Bank only)      | –6.0        | —   | —           | mA    | —     |
| <b>SSTL18 Class II</b>                              |  |             |     |             |       |       |
| VOH   | DC output logic High                                   | VTT + 0.603 | —   | —           | V     | —     |
| VOL   | DC output logic Low                                    | —           | —   | VTT – 0.603 | V     | —     |
| IOH at VOH  | Output minimum source DC current (DDRIO I/O Bank only) | 12.0        | —   | —           | mA    | —     |
| IOL at VOL  | Output minimum sink current (DDRIO I/O Bank only)      | –12.0       | —   | —           | mA    | —     |
| <b>SSTL18 DC Differential Voltage Specification</b> |  |             |     |             |       |       |
| VID (DC)  | DC input differential voltage                          | 0.3         | —   | —           | V     | —     |

**TABLE 2-50: SSTL18 AC SPECIFICATIONS (APPLICABLE TO DDRIO BANK ONLY)**

| Symbols   | Parameters  | Conditions                          | Min                | Typ         | Max                | Units |
|---|---|-------------------------------------|--------------------|-------------|--------------------|-------|
| <b>SSTL18 AC Differential Voltage Specification</b> |   |                                     |                    |             |                    |       |
| VDIFF (AC)  | AC input differential voltage   | —                                   | 0.5                | —           | —                  | V     |
| Vx (AC)   | AC differential cross point voltage   | —                                   | 0.5 × VDDI – 0.175 | —           | 0.5 × VDDI + 0.175 | V     |
| <b>SSTL18 Maximum AC Switching Speed</b>            |   |                                     |                    |             |                    |       |
| Dmax  | Maximum data rate (for DDRIO I/O Bank)  | AC loading: per JEDEC specification | —                  | —           | 600                | Mbps  |
| <b>SSTL18 Impedance Specifications</b>              |   |                                     |                    |             |                    |       |
| Rref  | Supported output driver calibrated impedance (for DDRIO I/O Bank)   | Reference resistor = 150Ω           | —                  | 20, 42      | —                  | Ω     |
| RTT   | Effective impedance value (ODT)   | Reference resistor = 150 Ω          | —                  | 50, 75, 150 | —                  | Ω     |
| <b>SSTL18 AC Test Parameters Specifications</b>     |   |                                     |                    |             |                    |       |
| Vtrip   | Measuring/trip point for data path  | —                                   | —                  | 0.9         | —                  | V     |
| Rent  | Resistance for enable path (t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> )         | —                                   | —                  | 2k          | —                  | Ω     |
| Cent  | Capacitive loading for enable path (t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> ) | —                                   | —                  | 5           | —                  | pF    |

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**TABLE 2-50: SSTL18 AC SPECIFICATIONS (APPLICABLE TO DDRIO BANK ONLY) (CONTINUED)**

| Symbols  | Parameters   | Conditions | Min | Typ | Max | Units    |
|----------|--|------------|-----|-----|-----|----------|
| Rtt_test | Reference resistance for data test path for SSTL18 Class I ( $t_{DP}$ )  | —          | —   | 50  | —   | $\Omega$ |
| Rtt_test | Reference resistance for data test path for SSTL18 Class II ( $t_{DP}$ ) | —          | —   | 25  | —   | $\Omega$ |
| Cload    | Capacitive loading for data path ( $t_{DP}$ )                            | —          | —   | 5   | —   | pF       |

#### 2.7.4.2 AC Switching Characteristics

##### 2.7.4.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-51: SSTL18 AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.71\text{V}$** 

|   | On-Die Termination (ODT) in $\Omega$ | Speed Grade -1 |    | Units |
|---|--------------------------------------|----------------|----|-------|
|   |                                      | $t_{PY}$       |    |       |
| <b>SSTL18 (for DDRIO I/O Bank with Fixed Codes)</b> |                                      |                |    |       |
| Pseudo differential                                 | None                                 | 1.641          | ns |       |
| True differential                                   | None                                 | 1.659          | ns |       |

##### 2.7.4.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-52: SSTL18 AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.71\text{V}$** 

|   | Speed Grade -1 |          |          |          |          | Units |
|---|----------------|----------|----------|----------|----------|-------|
|   | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| <b>SSTL18 Class I (for DDRIO I/O Bank)</b>  |                |          |          |          |          |       |
| Single Ended                                | 2.698          | 3.111    | 3.105    | 3.311    | 3.317    | ns    |
| Differential                                | 2.673          | 2.457    | 2.46     | 5.363    | 4.964    | ns    |
| <b>SSTL18 Class II (for DDRIO I/O Bank)</b> |                |          |          |          |          |       |
| Single Ended                                | 2.591          | 3.004    | 2.997    | 3.33     | 3.334    | ns    |
| Differential                                | 2.558          | 2.427    | 2.423    | 4.488    | 4.131    | ns    |

#### 2.7.5 STUB-SERIES TERMINATED LOGIC 1.5V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO 2 FPGAs. IGLOO 2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

##### 2.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

The following tables list the minimum and maximum AC/DC input and output levels specification.

**TABLE 2-53: SSTL15 DC VOLTAGE SPECIFICATION (FOR DDRIO I/O BANK ONLY)**

| Symbols  | Parameters                       | Min                                | Typ   | Max        | Units |  |  |  |
|--|----------------------------------|------------------------------------|-------|------------|-------|--|--|--|
| <b>Recommended DC Operating Conditions</b>       |                                  |                                    |       |            |       |  |  |  |
| VDDI   | Supply voltage                   | 1.425                              | 1.5   | 1.575      | V     |  |  |  |
| VTT  | Termination voltage              | 0.698                              | 0.750 | 0.803      | V     |  |  |  |
| VREF   | Input reference voltage          | 0.698                              | 0.750 | 0.803      | V     |  |  |  |
| <b>SSTL15 DC Input Voltage Specification</b>     |                                  |                                    |       |            |       |  |  |  |
| VIH(DC)  | DC input logic High              | VREF + 0.1                         | —     | 1.575      | V     |  |  |  |
| VIL(DC)  | DC input logic Low               | -0.3                               | —     | VREF - 0.1 | V     |  |  |  |
| IIH (DC)   | Input current High               | Refer to <a href="#">Table 2-3</a> |       |            | —     |  |  |  |
| IIL (DC)   | Input current Low                | Refer to <a href="#">Table 2-3</a> |       |            | —     |  |  |  |
| <b>SSTL15 DC Output Voltage Specification</b>    |                                  |                                    |       |            |       |  |  |  |
| <b>SSTL15 Class I</b>                            |                                  |                                    |       |            |       |  |  |  |
| VOH  | DC output logic High             | 0.8 x VDDI                         | —     | —          | V     |  |  |  |
| VOL  | DC output logic Low              | —                                  | —     | 0.2 x VDDI | V     |  |  |  |
| IOH at VOH                                       | Output minimum source DC current | 6.5                                | —     | —          | mA    |  |  |  |
| IOL at VOL                                       | Output minimum sink current      | -6.5                               | —     | —          | mA    |  |  |  |
| <b>SSTL15 Class II</b>                           |                                  |                                    |       |            |       |  |  |  |
| VOH  | DC output logic High             | 0.8 × VDDI                         | —     | —          | V     |  |  |  |
| VOL  | DC output logic Low              | —                                  | —     | 0.2 × VDDI | V     |  |  |  |
| IOH at VOH                                       | Output minimum source DC current | 7.6                                | —     | —          | mA    |  |  |  |
| IOL at VOL                                       | Output minimum sink current      | -7.6                               | —     | —          | mA    |  |  |  |
| <b>SSTL15 Differential Voltage Specification</b> |                                  |                                    |       |            |       |  |  |  |
| VID  | DC input differential voltage    | 0.2                                | —     | —          | V     |  |  |  |

**TABLE 2-54: SSTL15 AC SPECIFICATIONS**

| Symbols   | Parameters                                   | Conditions                           | Min                   | Typ                       | Max                   | Units |
|---|--|--------------------------------------|-----------------------|---------------------------|-----------------------|-------|
| <b>SSTL15 AC Differential Voltage Specification</b>                 |  |                                      |                       |                           |                       |       |
| VDIFF   | AC input differential voltage                | —                                    | 0.3                   | —                         | —                     | V     |
| Vx  | AC differential cross point voltage          | —                                    | 0.5 × VDDI<br>- 0.150 | —                         | 0.5 × VDDI<br>+ 0.150 | V     |
| <b>SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)</b> |  |                                      |                       |                           |                       |       |
| Dmax  | Maximum data rate                            | AC loading: per JEDEC specifications | —                     | —                         | 600                   | Mbps  |
| <b>SSTL15 AC Calibrated Impedance Option</b>                        |  |                                      |                       |                           |                       |       |
| Rref  | Supported output driver calibrated impedance | Reference resistor = 240Ω            | —                     | 34, 40                    | —                     | Ω     |
| RTT   | Effective impedance value (ODT)              | Reference resistor = 240Ω            | —                     | 20, 30,<br>40, 60,<br>120 | —                     | Ω     |
| <b>SSTL15 AC Test Parameters Specifications</b>                     |  |                                      |                       |                           |                       |       |

**TABLE 2-54: SSTL15 AC SPECIFICATIONS (CONTINUED)**

| Symbols  | Parameters   | Conditions | Min | Typ  | Max | Units    |
|----------|--|------------|-----|------|-----|----------|
| Vtrip    | Measuring/trip point for data path   | —          | —   | 0.75 | —   | V        |
| Rent     | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | —          | —   | 2k   | —   | $\Omega$ |
| Cent     | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | —          | —   | 5    | —   | pF       |
| Rtt_test | Reference resistance for data test path for SSTL15 Class I ( $t_{DP}$ )          | —          | —   | 50   | —   | $\Omega$ |
| Rtt_test | Reference resistance for data test path for SSTL15 Class II ( $t_{DP}$ )         | —          | —   | 25   | —   | $\Omega$ |
| Cload    | Capacitive loading for data path ( $t_{DP}$ )                                    | —          | —   | 5    | —   | pF       |

## 2.7.5.2 AC Switching Characteristics

## 2.7.5.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-55: SSTL15 AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.425\text{V}$** 

|  | ODT (On Die Termination)<br>in $\Omega$ | Speed Grade<br>-1 |  | Units |
|--|---|-------------------|--|-------|
|  |   | $t_{PY}$          |  |       |
| <b>SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only</b> |   |                   |  |       |
| Pseudo-Differential  | None                                    | 2.71              |  | ns    |
| True-Differential  | None                                    | 1.705             |  | ns    |

## 2.7.5.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-56: SSTL15 AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 1.425\text{V}$** 

|   | Speed Grade<br>-1 |          |          |          |          | Units |
|---|-------------------|----------|----------|----------|----------|-------|
|   | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| <b>SSTL15 Class I (for DDRIO I/O Bank)</b>  |                   |          |          |          |          |       |
| Single Ended                                | 2.861             | 2.796    | 2.797    | 4.5      | 3.996    | ns    |
| Differential                                | 2.85              | 2.882    | 2.877    | 3.379    | 2.813    | ns    |
| <b>SSTL15 Class II (for DDRIO I/O Bank)</b> |                   |          |          |          |          |       |
| Single Ended                                | 2.862             | 2.789    | 2.789    | 4.534    | 3.953    | ns    |
| Differential                                | 2.847             | 2.847    | 2.871    | 3.385    | 2.816    | ns    |

## 2.8 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microchip Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

### 2.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

#### 2.8.1.1 Minimum and Maximum Input and Output Levels

The following table lists the minimum and maximum input and output levels specification.

**TABLE 2-57: LVDS DC VOLTAGE SPECIFICATION**

| Symbols   | Parameters                        | Conditions | Min                | Typ   | Max   | Units |
|---|-----------------------------------|------------|--------------------|-------|-------|-------|
| <b>LVDS Recommended DC Operating Conditions</b> |                                   |            |                    |       |       |       |
| VDDI  | Supply voltage                    | 2.5V range | 2.375              | 2.5   | 2.625 | V     |
| VDDI  | Supply voltage                    | 3.3V range | 3.15               | 3.3   | 3.45  | V     |
| <b>LVDS DC Input Voltage Specification</b>      |                                   |            |                    |       |       |       |
| VI  | DC Input voltage                  | 2.5V range | 0                  | —     | 2.925 | V     |
| VI  | DC input voltage                  | 3.3V range | 0                  | —     | 3.45  | V     |
| IIH (DC)  | Input current High                | —          | Refer to Table 2-3 |       |       | —     |
| IIL (DC)  | Input current Low                 | —          | Refer to Table 2-3 |       |       | —     |
| <b>LVDS DC Output Voltage Specification</b>     |                                   |            |                    |       |       |       |
| VOH   | DC output logic High              | —          | 1.25               | 1.425 | 1.6   | V     |
| VOL   | DC output logic Low               | —          | 0.9                | 1.075 | 1.25  | V     |
| <b>LVDS Differential Voltage Specification</b>  |                                   |            |                    |       |       |       |
| VOD   | Differential output voltage swing | —          | 250                | 350   | 450   | mV    |
| VOCM  | Output common mode voltage        | —          | 1.125              | 1.25  | 1.375 | V     |
| VICM  | Input common mode voltage         | —          | 0.05               | 1.25  | 2.35  | V     |
| VID <sup>1</sup>                                | Input differential voltage        | —          | 100                | 350   | 600   | mV    |

- When VID is < 300 mV, the input signal is delayed by up to an additional 450 ps for LVDS25 and 280 ps for LVDS33. This delay is not accounted in the timing model. Clock insertion delays, propagation delays, and I/O to FF delays are marginally affected. Adding a parallel termination resistor of 200 Ω +/- 5% across the receiver pins can mitigate this additional delay when VID is < 300 mV.

**TABLE 2-58: LVDS AC SPECIFICATIONS**

| Symbols                                       | Parameters                             | Conditions                                | Min | Typ         | Max | Units |
|---|--|---|-----|-------------|-----|-------|
| <b>LVDS Maximum AC Switching Speed</b>        |  |   |     |             |     |       |
| Dmax  | Maximum data rate (for MSIO I/O Bank)  | AC loading: 12 pF/100 Ω differential load | —   | —           | 480 | Mbps  |
| Dmax  | Maximum data rate (for MSIOD I/O Bank) | AC loading: 10 pF/100 Ω differential load | —   | —           | 480 | Mbps  |
| <b>LVDS Impedance Specification</b>           |  |   |     |             |     |       |
| Rt  | Termination resistance                 | —   | —   | 100         | —   | Ω     |
| <b>LVDS AC Test Parameters Specifications</b> |  |   |     |             |     |       |
| Vtrip   | Measuring/trip point for data path     | —   | —   | Cross point | —   | V     |

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**TABLE 2-58: LVDS AC SPECIFICATIONS (CONTINUED)**

|      |  |   |   |    |   |          |
|------|--|---|---|----|---|----------|
| Rent | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | — | — | 2k | — | $\Omega$ |
| Cent | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | — | — | 5  | — | pF       |

## 2.8.1.2 LVDS25 AC Switching Characteristics

## 2.8.1.2.1 AC Switching Characteristics for Receiver (Input Buffers)

**TABLE 2-59: LVDS25 RECEIVER CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V, VDDI = 2.375V**

|                           | On-Die Termination (ODT) in $\Omega$ | Speed Grade -1 |    | Units |
|---------------------------|--------------------------------------|----------------|----|-------|
|                           |                                      | $t_{PY}$       |    |       |
| LVDS (for MSIO I/O Bank)  | None                                 | 3.085          | ns |       |
|                           | 100                                  | 3.081          | ns |       |
| LVDS (for MSIOD I/O Bank) | None                                 | 2.814          | ns |       |
|                           | 100                                  | 2.809          | ns |       |

## 2.8.1.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**TABLE 2-60: LVDS25 TRANSMITTER CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V, VDDI = 2.375V**

|                           | Speed Grade -1 |          |          |          |          | Units |
|---------------------------|----------------|----------|----------|----------|----------|-------|
|                           | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| LVDS (for MSIO I/O Bank)  | 2.324          | 2.63     | 2.617    | 2.466    | 2.382    | ns    |
| LVDS (for MSIOD I/O Bank) |                |          |          |          |          |       |
| No pre-emphasis           | 1.675          | 1.865    | 1.858    | 2.264    | 2.135    | ns    |
| Min pre-emphasis          | 1.6            | 1.889    | 1.886    | 2.295    | 2.169    | ns    |
| Med pre-emphasis          | 1.576          | 1.914    | 1.907    | 2.329    | 2.195    | ns    |

## 2.8.1.3 LVDS33 AC Switching Characteristics

## 2.8.1.3.1 AC Switching Characteristics for Receiver (Input Buffers)

**TABLE 2-61: LVDS33 RECEIVER CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V, VDDI = 3.15V**

|                            | On Die Termination (ODT) in $\Omega$ | Speed Grade -1 |    | Units |
|----------------------------|--------------------------------------|----------------|----|-------|
|                            |                                      | $t_{PY}$       |    |       |
| LVDS33 (for MSIO I/O Bank) | None                                 | 2.784          | ns |       |
|                            | 100                                  | 2.781          | ns |       |

## 2.8.1.3.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-62: LVDS33 TRANSMITTER CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE  
1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 3.15\text{V}$**

|                            | Speed Grade<br>-1 |          |          |          |          | Units |
|----------------------------|-------------------|----------|----------|----------|----------|-------|
|                            | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| LVDS33 (for MSIO I/O Bank) | 2.091             | 2.134    | 2.128    | 2.154    | 2.092    | ns    |

## 2.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

### 2.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

The following tables list the minimum and maximum input and output levels specification. s

**TABLE 2-63: B-LVDS DC VOLTAGE SPECIFICATION**

| Symbols  | Parameters   | Min                                | Typ   | Max   | Units |
|--|--|------------------------------------|-------|-------|-------|
| <b>Bus-LVDS Recommended DC Operating Conditions</b>                      |  |                                    |       |       |       |
| VDDI   | Supply voltage   | 2.375                              | 2.5   | 2.625 | V     |
| <b>Bus-LVDS DC Input Voltage Specification</b>                           |  |                                    |       |       |       |
| VI   | DC input voltage   | 0                                  | —     | 2.925 | V     |
| IIH (DC)   | Input current High   | Refer to <a href="#">Table 2-3</a> |       |       |       |
| IIL (DC)   | Input current Low  | Refer to <a href="#">Table 2-3</a> |       |       |       |
| <b>Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)</b> |  |                                    |       |       |       |
| VOH  | DC output logic High                                       | 1.25                               | 1.425 | 1.6   | V     |
| VOL  | DC output logic Low  | 0.9                                | 1.075 | 1.25  | V     |
| <b>Bus-LVDS Differential Voltage Specification</b>                       |  |                                    |       |       |       |
| VOD  | Differential output voltage swing (for MSIO I/O Bank only) | 65                                 | —     | 460   | mV    |
| VOCM   | Output common mode voltage (for MSIO I/O Bank only)        | 1.1                                | —     | 1.5   | V     |
| VICM   | Input common mode voltage                                  | 0.05                               | —     | 2.4   | V     |
| VID  | Input differential voltage                                 | 0.1                                | —     | VDDI  | V     |

**TABLE 2-64: B-LVDS AC SPECIFICATIONS**

| Symbols   | Parameters                            | Conditions                                      | Min | Typ         | Max | Units    |
|---|---------------------------------------|---|-----|-------------|-----|----------|
| <b>Bus-LVDS Maximum AC Switching Speed</b>        |                                       |   |     |             |     |          |
| Dmax  | Maximum data rate (for MSIO I/O Bank) | AC loading: 2 pF/100 $\Omega$ differential load | —   | —           | 450 | Mbps     |
| <b>Bus-LVDS Impedance Specifications</b>          |                                       |   |     |             |     |          |
| Rt  | Termination resistance                | —   | —   | 27          | —   | $\Omega$ |
| <b>Bus-LVDS AC Test Parameters Specifications</b> |                                       |   |     |             |     |          |
| Vtrip   | Measuring/trip point for data path    | —   | —   | Cross point | —   | V        |

**TABLE 2-64: B-LVDS AC SPECIFICATIONS (CONTINUED)**

|      |   |   |   |    |   |          |
|------|---|---|---|----|---|----------|
| Rent | Resistance for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | — | — | 2k | — | $\Omega$ |
| Cent | Capacitive loading for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | — | — | 5  | — | pF       |

## 2.8.2.2 AC Switching Characteristics

## 2.8.2.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-65: B-LVDS AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 2.375\text{V}$** 

|                               | On-Die Termination (ODT) in $\Omega$ | Speed Grade<br>-1 | Units |
|-------------------------------|--------------------------------------|-------------------|-------|
|                               |                                      | $t_{PY}$          |       |
| Bus-LVDS (for MSIO I/O Bank)  | None                                 | 3.036             | ns    |
|                               | 100                                  | 3.031             | ns    |
| Bus-LVDS (for MSIOD I/O Bank) | None                                 | 2.744             | ns    |
|                               | 100                                  | 2.747             | ns    |

## 2.8.2.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-66: B-LVDS AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 2.375\text{V}$** 

|                              | Speed Grade<br>-1 |          |          |          |          | Units |
|------------------------------|-------------------|----------|----------|----------|----------|-------|
|                              | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| Bus-LVDS (for MSIO I/O Bank) | 2.81              | 2.66     | 2.645    | 2.477    | 2.537    | ns    |

## 2.8.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

## 2.8.3.1 Minimum and Maximum Input and Output Levels

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-67: M-LVDS DC VOLTAGE SPECIFICATION**

| Symbols  | Parameters         | Min                | Typ | Max   | Units | Notes |
|--|--------------------|--------------------|-----|-------|-------|-------|
| <b>M-LVDS Recommended DC Operating Conditions</b>                      |                    |                    |     |       |       |       |
| VDDI   | Supply voltage     | 2.375              | 2.5 | 2.625 | V     | *     |
| <b>M-LVDS DC Input Voltage Specification</b>                           |                    |                    |     |       |       |       |
| VI   | DC input voltage   | 0                  | —   | 2.925 | V     | —     |
| IIH (DC)   | Input current High | Refer to Table 2-3 |     |       | —     | —     |
| IIL (DC)   | Input current Low  | Refer to Table 2-3 |     |       | —     | —     |
| <b>M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)</b> |                    |                    |     |       |       |       |

**TABLE 2-67: M-LVDS DC VOLTAGE SPECIFICATION (CONTINUED)**

| Symbols  | Parameters   | Min  | Typ   | Max  | Units | Notes |
|--|--|------|-------|------|-------|-------|
| VOH  | DC output logic High                                       | 1.25 | 1.425 | 1.6  | V     | —     |
| VOL  | DC output logic Low  | 0.9  | 1.075 | 1.25 | V     | —     |
| <b>M-LVDS Differential Voltage Specification</b> |  |      |       |      |       |       |
| VOD  | Differential output voltage Swing (for MSIO I/O Bank only) | 300  | —     | 650  | mV    | —     |
| VOCM   | Output common mode voltage (for MSIO I/O Bank only)        | 0.3  | —     | 2.1  | V     | —     |
| VICM   | Input common mode voltage                                  | 0.3  | —     | 1.2  | V     | —     |
| VID  | Input differential voltage                                 | 50   | —     | 2400 | mV    | —     |
| <b>Note:</b> *Only M-LVDS TYPE I is supported.   |  |      |       |      |       |       |

**TABLE 2-68: M-LVDS AC SPECIFICATIONS**

| Symbols   | Parameters  | Conditions                                 | Min | Typ         | Max | Units |
|---|---|--|-----|-------------|-----|-------|
| <b>M-LVDS Maximum AC Switching Speeds</b>       |   |  |     |             |     |       |
| Dmax  | Maximum data rate (for MSIO I/O Bank)                   | AC loading: 2 pF / 100 Ω differential load | —   | —           | 450 | Mbps  |
| <b>M-LVDS Impedance Specification</b>           |   |  |     |             |     |       |
| Rt  | Termination resistance                                  | —  | —   | 50          | —   | Ω     |
| <b>M-LVDS AC Test Parameters Specifications</b> |   |  |     |             |     |       |
| VTrip   | Measuring/trip point for data path                      | —  | —   | Cross point | —   | V     |
| Rent  | Resistance for enable path (tZH, tZL, tHZ, tLZ)         | —  | —   | 2k          | —   | Ω     |
| Cent  | Capacitive loading for enable path (tZH, tZL, tHZ, tLZ) | —  | —   | 5           | —   | pF    |

### 2.8.3.2 AC Switching Characteristics

#### 2.8.3.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-69: M-LVDS AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS: T<sub>J</sub> = 135 °C, VDD = 1.14V, VDDI= 2.375V**

|                             | On-Die Termination (ODT) in Ω | Speed Grade |                  | Units |
|-----------------------------|-------------------------------|-------------|------------------|-------|
|                             |                               | -1          | t <sub>PDY</sub> |       |
| M-LVDS (for MSIO I/O Bank)  | None                          | 3.036       | ns               |       |
|                             | 100                           | 3.031       | ns               |       |
| M-LVDS (for MSIOD I/O Bank) | None                          | 2.744       | ns               |       |
|                             | 100                           | 2.747       | ns               |       |

#### 2.8.3.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-70: M-LVDS AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 2.375\text{V}$**

|                            | Speed Grade<br>-1 |          |          |          |          | Units |
|----------------------------|-------------------|----------|----------|----------|----------|-------|
|                            | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| M-LVDS (for MSIO I/O Bank) | 2.81              | 2.66     | 2.644    | 2.539    | 2.455    | ns    |

## 2.8.4 MINI-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

### 2.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-71: MINI-LVDS DC VOLTAGE SPECIFICATION**

| Symbols   | Parameters                        | Min   | Typ   | Max   | Units |
|---|-----------------------------------|-------|-------|-------|-------|
| <b>Recommended DC Operating Conditions</b>          |                                   |       |       |       |       |
| VDDI  | Supply voltage                    | 2.375 | 2.5   | 2.625 | V     |
| <b>Mini-LVDS DC Input Voltage Specification</b>     |                                   |       |       |       |       |
| VI  | DC Input voltage                  | 0     | —     | 2.925 | V     |
| <b>Mini-LVDS DC Output Voltage Specification</b>    |                                   |       |       |       |       |
| VOH   | DC output logic High              | 1.25  | 1.425 | 1.6   | V     |
| VOL   | DC output logic Low               | 0.9   | 1.075 | 1.25  | V     |
| <b>Mini-LVDS Differential Voltage Specification</b> |                                   |       |       |       |       |
| VOD   | Differential output voltage swing | 300   | —     | 600   | mV    |
| VOCM  | Output common mode voltage        | 1     | —     | 1.4   | V     |
| VICM  | Input common mode voltage         | 0.3   | —     | 1.2   | V     |
| VID   | Input differential voltage        | 100   | —     | 600   | mV    |

**TABLE 2-72: MINI-LVDS AC SPECIFICATIONS**

| Symbols  | Parameters                         | Conditions                                | Min | Typ         | Max | Units |
|--|------------------------------------|---|-----|-------------|-----|-------|
| <b>Mini-LVDS Maximum AC Switching Speed</b>        |                                    |   |     |             |     |       |
| Dmax   | Maximum data rate (MSIO I/O Bank)  | AC loading: 2 pF/100 Ω differential load  | —   | —           | 460 | Mbps  |
| Dmax   | Maximum data rate (MSIOD I/O Bank) | AC loading: 10 pF/100 Ω differential load | —   | —           | 480 | Mbps  |
| <b>Mini-LVDS Impedance Specification</b>           |                                    |   |     |             |     |       |
| Rt   | Termination resistance             | —   | —   | 100         | —   | Ω     |
| <b>Mini-LVDS AC Test Parameters Specifications</b> |                                    |   |     |             |     |       |
| VTrip  | Measuring/trip point for data path | —   | —   | Cross point | —   | V     |

**TABLE 2-72: MINI-LVDS AC SPECIFICATIONS (CONTINUED)**

|      |   |   |   |    |   |          |
|------|---|---|---|----|---|----------|
| Rent | Resistance for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | — | — | 2k | — | $\Omega$ |
| Cent | Capacitive loading for enable path<br>( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | — | — | 5  | — | pF       |

## 2.8.4.2 AC Switching Characteristics

2.8.4.2.1 *AC Switching Characteristics for Receiver (Input Buffers)*

The following table lists the AC switching characteristics for receiver.

**TABLE 2-73: MINI-LVDS AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V, VDDI = 2.375V**

|                                | On-Die Termination (ODT) in $\Omega$ | Speed Grade | Units |
|--------------------------------|--------------------------------------|-------------|-------|
|                                |                                      | -1          |       |
| Mini-LVDS (for MSIO I/O Bank)  | None                                 | 3.137       | ns    |
|                                | 100                                  | 3.132       | ns    |
| Mini-LVDS (for MSIOD I/O Bank) | None                                 | 2.945       | ns    |
|                                | 100                                  | 2.934       | ns    |

2.8.4.2.2 *AC Switching Characteristics for Transmitter (Output and Tristate Buffers)*

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-74: MINI-LVDS AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V, VDDI = 2.375V**

|                                       | Speed Grade |          |          |          |          | Units |
|---------------------------------------|-------------|----------|----------|----------|----------|-------|
|                                       | $t_{DP}$    | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| Mini-LVDS (for MSIO I/O Bank)         | 2.325       | 2.63     | 2.618    | 2.466    | 2.382    | ns    |
| <b>Mini-LVDS (for MSIOD I/O Bank)</b> |             |          |          |          |          |       |
| No pre-emphasis                       | 1.67        | 1.86     | 1.853    | 2.26     | 2.131    | ns    |
| Min pre-emphasis                      | 1.67        | 1.86     | 1.853    | 2.26     | 2.131    | ns    |
| Med pre-emphasis                      | 1.594       | 1.889    | 1.88     | 2.166    | 2.306    | ns    |
| Max pre-emphasis                      | 1.573       | 1.915    | 1.904    | 2.198    | 2.339    | ns    |

## 2.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

## 2.8.5.1 Minimum and Maximum Input and Output Levels

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-75: RSDS DC VOLTAGE SPECIFICATION**

| Symbols                                    | Parameters     | Min   | Typ | Max   | Units |
|--|----------------|-------|-----|-------|-------|
| <b>Recommended DC Operating Conditions</b> |                |       |     |       |       |
| VDDI                                       | Supply voltage | 2.375 | 2.5 | 2.625 | V     |

**TABLE 2-75: RSDS DC VOLTAGE SPECIFICATION (CONTINUED)**

| Symbols  | Parameters                        | Min  | Typ   | Max   | Units |
|--|-----------------------------------|------|-------|-------|-------|
| <b>RSDS DC Input Voltage Specification</b>     |                                   |      |       |       |       |
| VI   | DC input voltage                  | 0    | —     | 2.925 | V     |
| <b>RSDS DC Output Voltage Specification</b>    |                                   |      |       |       |       |
| VOH  | DC output logic High              | 1.25 | 1.425 | 1.6   | V     |
| VOL  | DC output logic Low               | 0.9  | 1.075 | 1.25  | V     |
| <b>RSDS Differential Voltage Specification</b> |                                   |      |       |       |       |
| VOD  | Differential output voltage swing | 100  | —     | 600   | mV    |
| VOCM   | Output common mode voltage        | 0.5  | —     | 1.5   | V     |
| VICM   | Input common mode voltage         | 0.3  | —     | 1.5   | V     |
| VID  | Input differential voltage        | 100  | —     | 600   | mV    |

**TABLE 2-76: RSDS AC SPECIFICATIONS**

| Symbols                                       | Parameters  | Conditions                                | Min | Typ         | Max | Units |
|---|---|---|-----|-------------|-----|-------|
| <b>RSDS Maximum AC Switching Speed</b>        |   |   |     |             |     |       |
| Dmax  | Maximum data rate<br>(for MSIO I/O Bank)  | AC loading: 2 pF/100 Ω differential load  | —   | —           | 460 | Mbps  |
| Dmax  | Maximum data rate<br>(for MSIOD I/O Bank)   | AC loading: 10 pF/100 Ω differential load | —   | —           | 480 | Mbps  |
| <b>RSDS Impedance Specification</b>           |   |   |     |             |     |       |
| Rt  | Termination resistance  | —   | —   | 100         | —   | Ω     |
| <b>RSDS AC Test Parameters Specifications</b> |   |   |     |             |     |       |
| VTrip   | Measuring/trip point for data path  | —   | —   | Cross point | —   | V     |
| Rent  | Resistance for enable path<br>(t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> )      | —   | —   | 2k          | —   | Ω     |
| Cent  | Capacitive loading for enable path (t <sub>ZH</sub> , t <sub>ZL</sub> , t <sub>HZ</sub> , t <sub>LZ</sub> ) | —   | —   | 5           | —   | pF    |

### 2.8.5.2 AC Switching Characteristics

#### 2.8.5.2.1 AC Switching Characteristics for Receiver (Input Buffers)

The following table lists the AC switching characteristics for receiver.

**TABLE 2-77: RSDS AC SWITCHING CHARACTERISTICS FOR RECEIVER (INPUT BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS: T<sub>J</sub> = 135 °C, V<sub>DD</sub> = 1.14V, V<sub>DDI</sub> = 2.375V**

|                           | On-Die Termination (ODT) in Ω | Speed Grade | Units |
|---------------------------|-------------------------------|-------------|-------|
|                           |                               | -1          |       |
| RSDS (for MSIO I/O Bank)  | None                          | 3.137       | ns    |
|                           | 100                           | 3.132       | ns    |
| RSDS (for MSIOD I/O Bank) | None                          | 2.855       | ns    |
|                           | 100                           | 2.844       | ns    |

#### 2.8.5.2.2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

The following table lists the AC switching characteristics for transmitter.

**TABLE 2-78: RSDS AC SWITCHING CHARACTERISTICS FOR TRANSMITTER (OUTPUT AND TRISTATE BUFFERS)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 2.375\text{V}$**

|                                  | Speed Grade<br>-1 |          |          |          |          | Units |
|----------------------------------|-------------------|----------|----------|----------|----------|-------|
|                                  | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| RSDS (for MSIO I/O Bank)         | 2.28              | 2.511    | 2.498    | 2.068    | 2.165    | ns    |
| <b>RSDS (for MSIOD I/O Bank)</b> |                   |          |          |          |          |       |
| No pre-emphasis                  | 1.678             | 1.665    | 1.662    | 1.626    | 1.706    | ns    |
| Min pre-emphasis                 | 1.669             | 1.859    | 1.852    | 2.132    | 2.27     | ns    |
| Med pre-emphasis                 | 1.593             | 1.888    | 1.879    | 2.166    | 2.306    | ns    |
| Max pre-emphasis                 | 1.572             | 1.913    | 1.902    | 2.198    | 2.339    | ns    |

## 2.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO 2 FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

### 2.8.6.1 Minimum and Maximum Input and Output Levels

The following tables list the minimum and maximum input and output levels specification.

**TABLE 2-79: LVPECL DC VOLTAGE SPECIFICATION (APPLICABLE TO MSIO I/O BANKS ONLY)**

| Symbols  | Parameters                 | Min  | Typ | Max   | Units |
|--|----------------------------|------|-----|-------|-------|
| <b>Recommended DC Operating Conditions</b>       |                            |      |     |       |       |
| VDDI   | Supply voltage             | 3.15 | 3.3 | 3.45  | V     |
| <b>LVPECL DC Input Voltage Specification</b>     |                            |      |     |       |       |
| VI   | DC input voltage           | 0    | —   | 3.45  | V     |
| <b>LVPECL Differential Voltage Specification</b> |                            |      |     |       |       |
| VICM   | Input common mode voltage  | 0.3  | —   | 2.8   | V     |
| VIDIFF   | Input differential voltage | 100  | 300 | 1,000 | mV    |

**TABLE 2-80: LVPECL MAXIMUM AC SWITCHING SPEEDS (APPLICABLE TO MSIO I/O BANKS ONLY)**

| Symbols                         | Parameters                            | Min | Typ | Max | Units |
|---------------------------------|---------------------------------------|-----|-----|-----|-------|
| <b>LVPECL AC Specifications</b> |                                       |     |     |     |       |
| Fmax                            | Maximum data rate (for MSIO I/O Bank) | —   | —   | 810 | Mbps  |

### 2.8.6.2 AC Switching Characteristics

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AC Switching Characteristics for Receiver (Input Buffers)

**TABLE 2-81: LVPECL RECEIVER CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1  
CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ ,  $VDDI = 3.15\text{V}$**

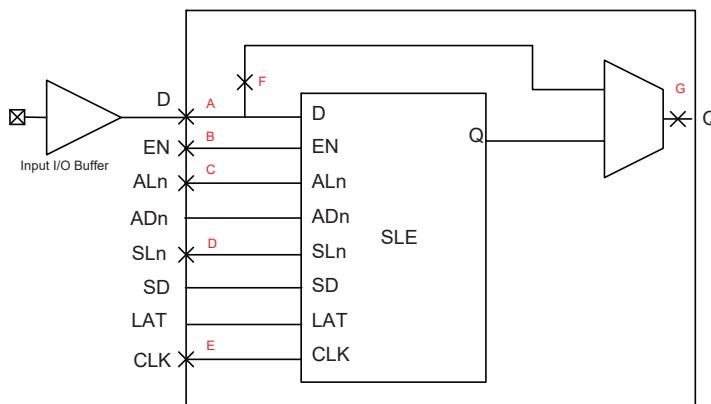
|                            | On-Die Termination (ODT) in $\Omega$ | $t_{PD}$          | Units |
|----------------------------|--------------------------------------|-------------------|-------|
|                            |                                      | Speed Grade<br>-1 |       |
| LVPECL (for MSIO I/O Bank) | None                                 | 2.784             | ns    |
|                            | 100                                  | 2.781             | ns    |

## 2.9 I/O Register Specifications

### 2.9.1 INPUT REGISTER

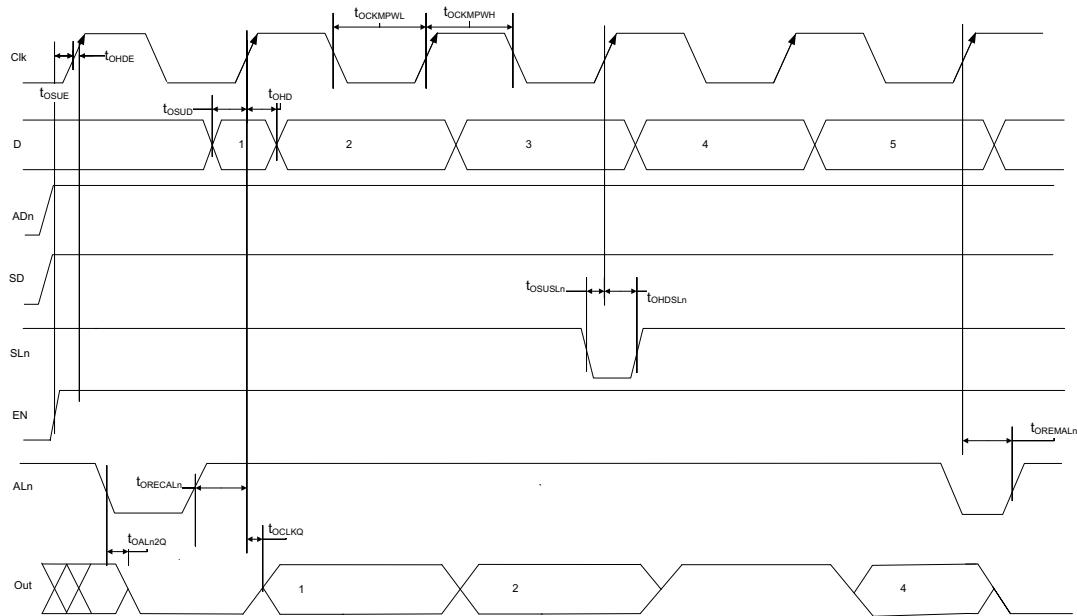
The following figure shows the timing model for input register.

**FIGURE 2-4: TIMING MODEL FOR INPUT REGISTER**



The following figure shows the I/O register input timing diagram.

**FIGURE 2-5: I/O REGISTER INPUT TIMING DIAGRAM.**



The following table lists the Input Data register propagation delays.

**TABLE 2-82: INPUT DATA REGISTER PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

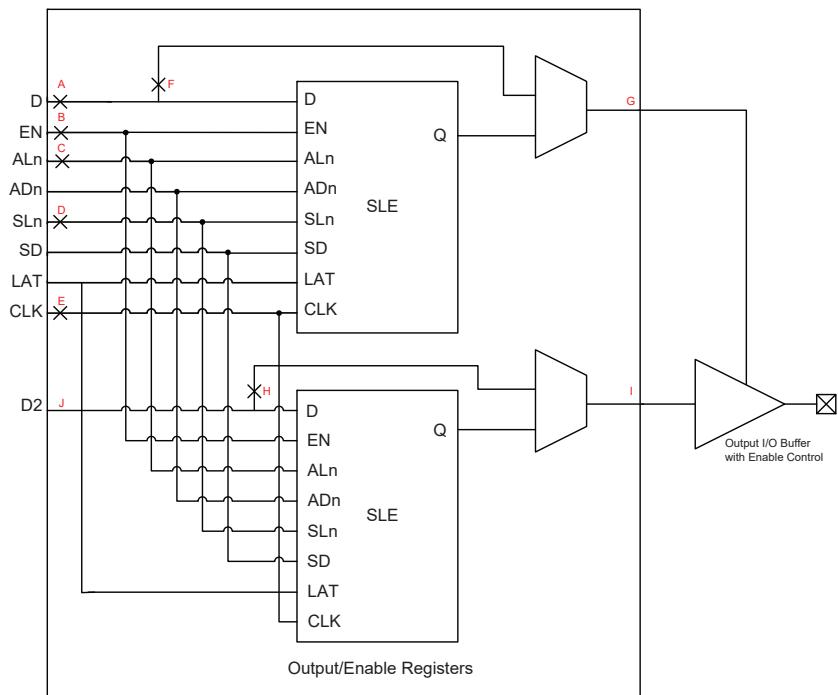
| Parameter      | Description  | Measuring Nodes (From, To)* | Speed Grade -1 | Units |
|----------------|--|-----------------------------|----------------|-------|
| $t_{IBYP}^1$   | Bypass Delay of the Input Register                           | F, G                        | —              | ns    |
| $t_{ICLKQ}$    | Clock-to-Q of the Input Register                             | E, G                        | 0.131          | ns    |
| $t_{ISUD}^1$   | Data Setup Time for the Input Register                       | A, E                        | —              | ns    |
| $t_{IHD}^1$    | Data Hold Time for the Input Register                        | A, E                        | —              | ns    |
| $t_{ISUE}$     | Enable Setup Time for the Input Register                     | B, E                        | 0.824          | ns    |
| $t_{IHE}$      | Enable Hold Time for the Input Register                      | B, E                        | 0.016          | ns    |
| $t_{ISUSL}$    | Synchronous Load Setup Time for the Input Register           | D, E                        | 1.733          | ns    |
| $t_{IHSL}$     | Synchronous Load Hold Time for the Input Register            | D, E                        | 0.062          | ns    |
| $t_{IALn2Q}$   | Asynchronous Clear-to-Q of the Input Register (ADn=1)        | C, G                        | 0.504          | ns    |
|                | Asynchronous Preset-to-Q of the Input Register (ADn=0)       | C, G                        | 0.461          | ns    |
| $t_{IREMALn}$  | Asynchronous Load Removal Time for the Input Register        | C, E                        | 0.128          | ns    |
| $t_{IRECALn}$  | Asynchronous Load Recovery Time for the Input Register       | C, E                        | 0.214          | ns    |
| $t_{IWALn}$    | Asynchronous Load Minimum Pulse Width for the Input Register | C, C                        | 0.446          | ns    |
| $t_{ICKMPWHL}$ | Clock Minimum Pulse Width High for the Input Register        | E, E                        | 0.101          | ns    |
| $t_{ICKMPWL}$  | Clock Minimum Pulse Width Low for the Input Register         | E, E                        | 0.223          | ns    |

1. Delay depends on the device and I/O location. Use the SmartTime tool in Libero for accurate timing data.

## 2.9.2 OUTPUT/ENABLE REGISTER

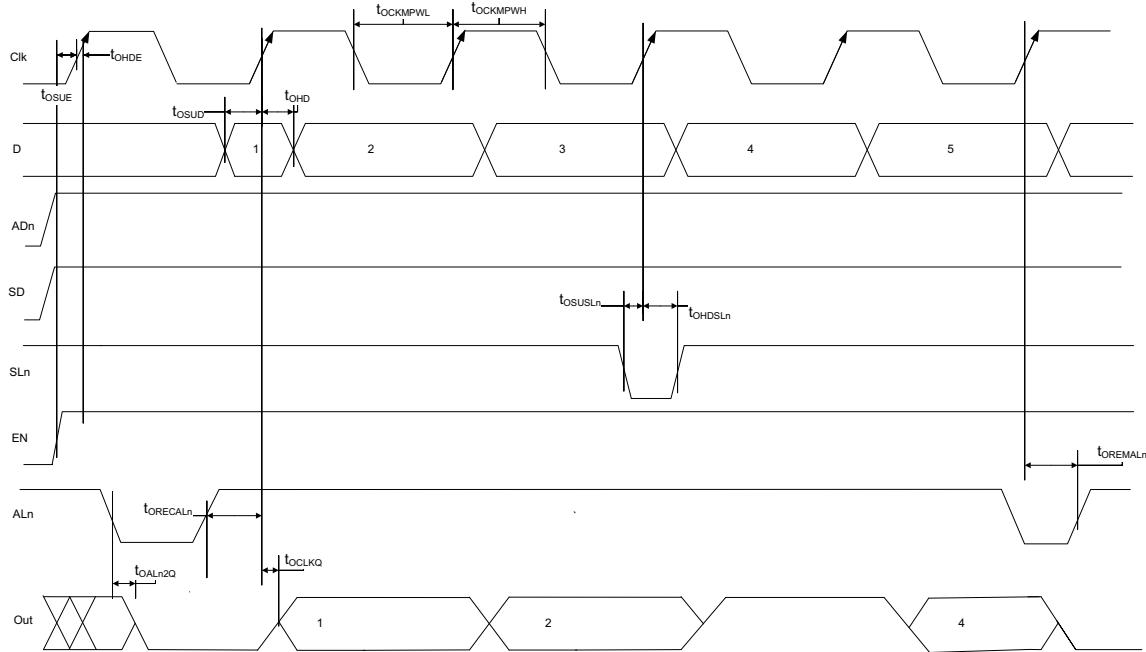
The following figure shows the Output/Enable register timing diagram.

**FIGURE 2-6: TIMING MODEL FOR OUTPUT/ENABLE REGISTER**



The following figure shows the I/O register output timing diagram.

**FIGURE 2-7: I/O REGISTER OUTPUT TIMING DIAGRAM**



The following table lists the Output/Enable Data register propagation delays.

**TABLE 2-83: OUTPUT/ENABLE DATA REGISTER PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter     | Description  | Measuring Nodes (From, To) | Speed Grade -1 | Units |
|---------------|--|----------------------------|----------------|-------|
| $t_{OBYP}$    | Bypass Delay of the Output/Enable Register                           | F, G or H, I               | 0.343          | ns    |
| $t_{OCLKQ}$   | Clock-to-Q of the Output/Enable Register                             | E, G or E, I               | 0.255          | ns    |
| $t_{OSUD}$    | Data Setup Time for the Output/Enable Register                       | A, E or J, E               | 0.27           | ns    |
| $t_{OHD}$     | Data Hold Time for the Output/Enable Register                        | A, E or J, E               | 0.037          | ns    |
| $t_{OSUE}$    | Enable Setup Time for the Output/Enable Register                     | B, E                       | 0.824          | ns    |
| $t_{OHE}$     | Enable Hold Time for the Output/Enable Register                      | B, E                       | 0.029          | ns    |
| $t_{OSUSL}$   | Synchronous Load Setup Time for the Output/Enable Register           | D, E                       | 1.831          | ns    |
| $t_{OHSL}$    | Synchronous Load Hold Time for the Output/Enable Register            | D, E                       | 0.062          | ns    |
| $t_{OALn2Q}$  | Asynchronous Clear-to-Q of the Output/Enable Register ( $ADn=1$ )    | C, G or C, I               | 0.561          | ns    |
|               | Asynchronous Preset-to-Q of the Output/Enable Register ( $ADn=0$ )   | C, G or C, I               | 0.528          | ns    |
| $t_{OREMALn}$ | Asynchronous Load Removal Time for the Output/Enable Register        | C, E                       | 0.134          | ns    |
| $t_{ORECALn}$ | Asynchronous Load Recovery Time for the Output/Enable Register       | C, E                       | 0.237          | ns    |
| $t_{OWALn}$   | Asynchronous Load Minimum Pulse Width for the Output/Enable Register | C, C                       | 0.446          | ns    |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output/Enable Register        | E, E                       | 0.101          | ns    |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output/Enable Register         | E, E                       | 0.223          | ns    |

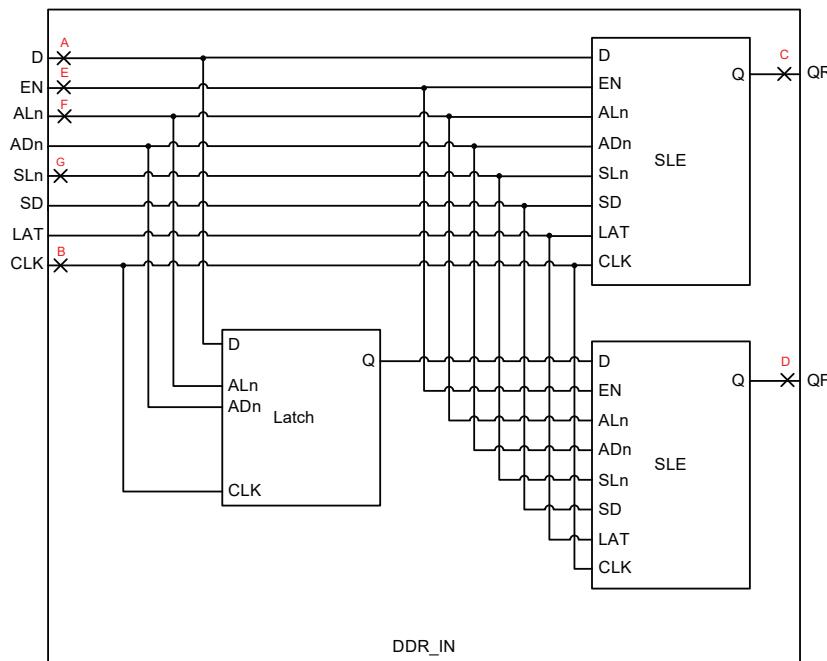
## 2.10 DDR Module Specification

### 2.10.1 INPUT DDR MODULE

The following figure shows the input DDR module.

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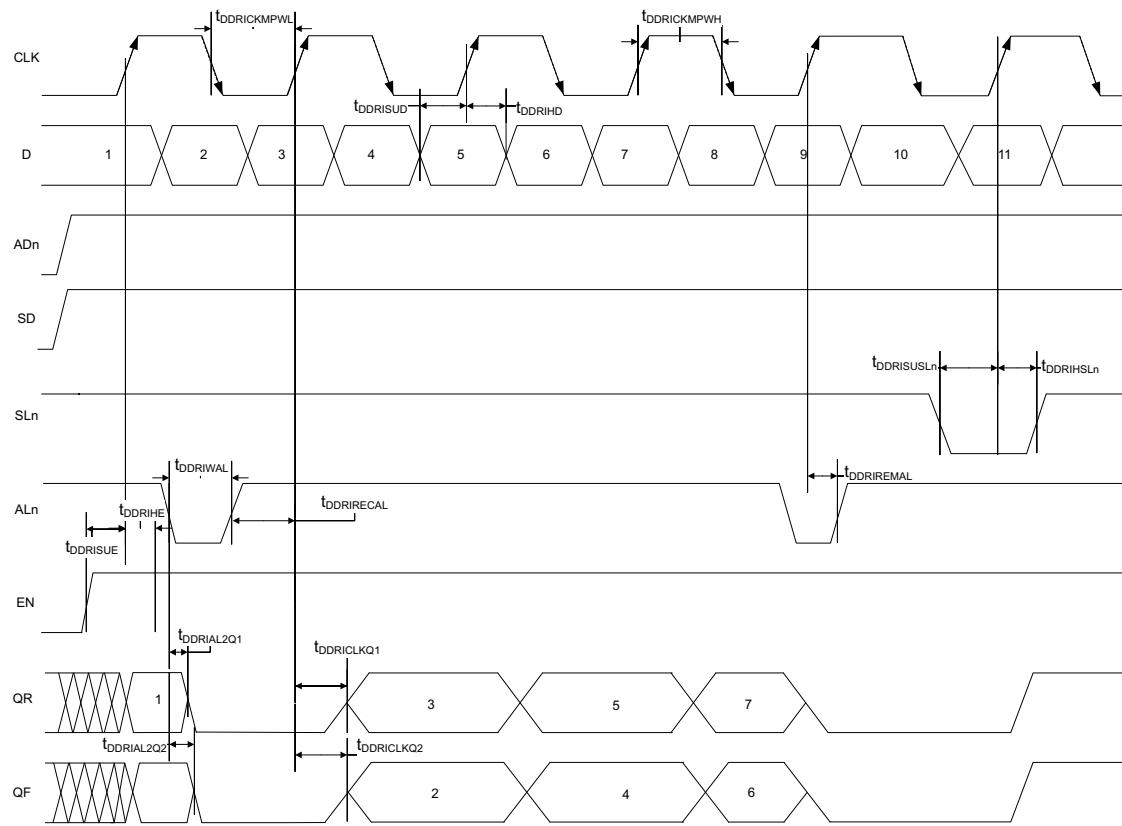
**FIGURE 2-8: INPUT DDR MODULE**



#### 2.10.2 INPUT DDR TIMING DIAGRAM

The following figure shows the input DDR timing diagram.

**FIGURE 2-9: INPUT DDR TIMING DIAGRAM**



### 2.10.3 TIMING CHARACTERISTICS

The following table lists the input DDR propagation delays.

**TABLE 2-84: INPUT DDR PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter         | Description   | Measuring Nodes (From, To) | Speed Grade -1 | Units |
|-------------------|---|----------------------------|----------------|-------|
| $t_{DDRICLKQ1}^1$ | Clock-to-Out Out_QR for Input DDR                   | B, C                       | 0.131          | ns    |
| $t_{DDRICLKQ2}$   | Clock-to-Out Out_QF for Input DDR                   | B, D                       | 0.131          | ns    |
| $t_{DDRISUD}^1$   | Data Setup for Input DDR                            | A, B                       |                | ns    |
| $t_{DDRIHD}^1$    | Data Hold for Input DDR                             | A, B                       |                | ns    |
| $t_{DDRISUE}$     | Enable Setup for Input DDR                          | E, B                       | 0.824          | ns    |
| $t_{DDRIHE}$      | Enable Hold for Input DDR                           | E, B                       | 0.016          | ns    |
| $t_{DDRISUSLn}$   | Synchronous Load Setup for Input DDR                | G, B                       | 1.733          | ns    |
| $t_{DDRIHSLn}$    | Synchronous Load Hold for Input DDR                 | G, B                       | 0.062          | ns    |
| $t_{DDRIAL2Q1}$   | Asynchronous Load-to-Out QR for Input DDR           | F, C                       | 0.461          | ns    |
| $t_{DDRIAL2Q2}$   | Asynchronous Load-to-Out QF for Input DDR           | F, D                       | 0.417          | ns    |
| $t_{DDRIREMAL}$   | Asynchronous Load Removal time for Input DDR        | F, B                       | 0.128          | ns    |
| $t_{DDRIRECAL}$   | Asynchronous Load Recovery time for Input DDR       | F, B                       | 0.214          | ns    |
| $t_{DDRIWAL}$     | Asynchronous Load Minimum Pulse Width for Input DDR | F, F                       | 0.446          | ns    |

**TABLE 2-84: INPUT DDR PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

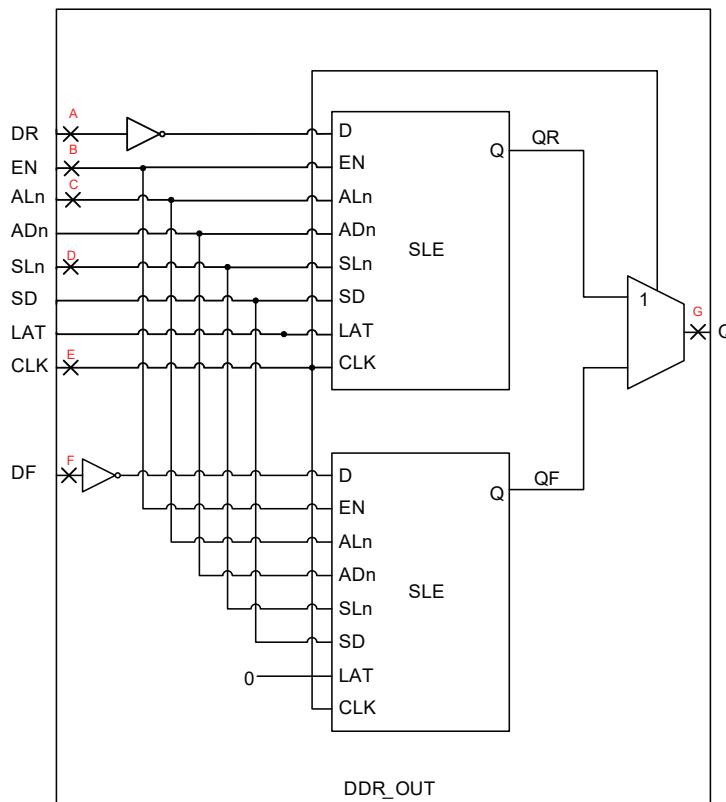
|                  |  |      |       |    |
|------------------|--|------|-------|----|
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width High for Input DDR | B, B | 0.101 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width Low for Input DDR  | B, B | 0.223 | ns |

1. Delay depends on the device and I/O location. Use the SmartTime tool in Libero for accurate timing data.

#### 2.10.4 OUTPUT DDR MODULE

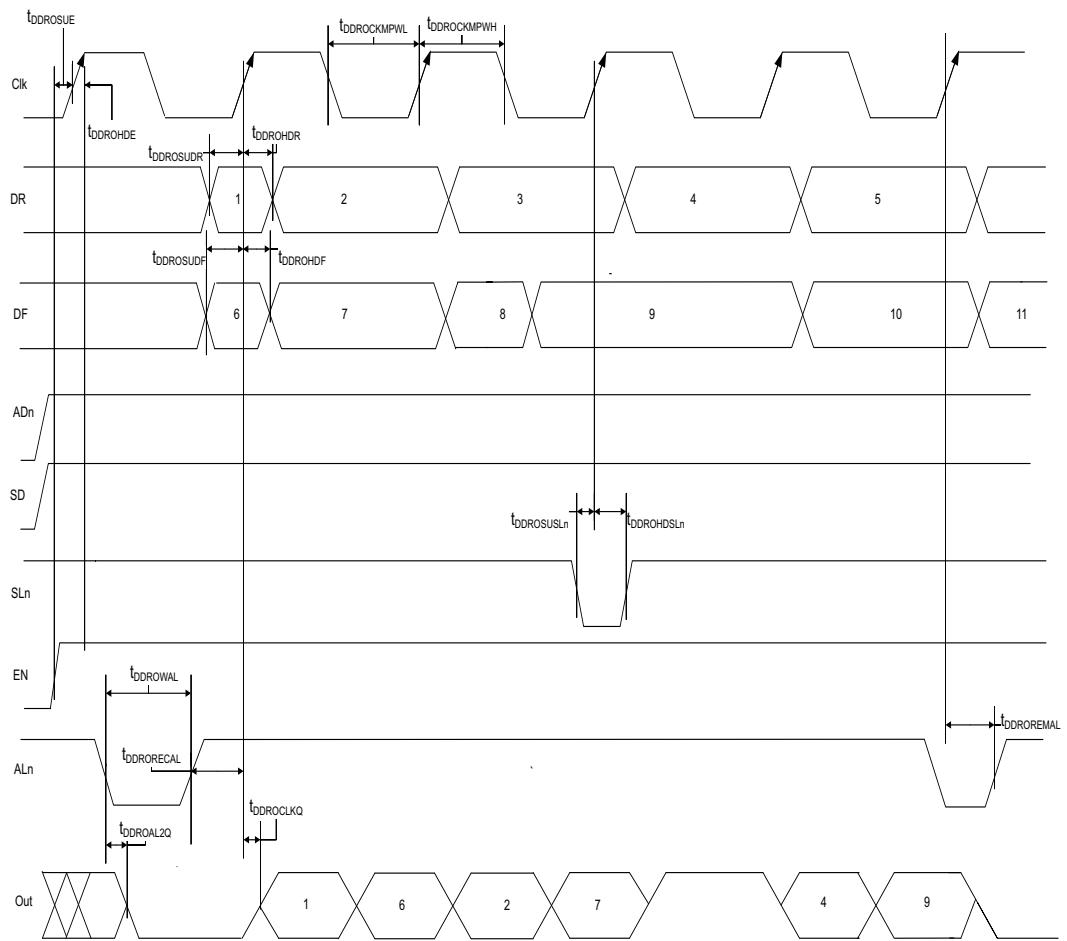
The following figure shows the output DDR module.

**FIGURE 2-10: OUTPUT DDR MODULE**



The following figure shows the output DDR timing diagram.

## **FIGURE 2-11: OUTPUT DDR TIMING DIAGRAM**



### 2.10.5 TIMING CHARACTERISTICS

The following table lists the timing characteristics.

**TABLE 2-85: OUTPUT DDR PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter        | Description                           | Measuring Nodes<br>(From, To) | Speed Grade<br>-1 | Units |
|------------------|---------------------------------------|-------------------------------|-------------------|-------|
| $t_{DDROCLKQ}$   | Clock-to-Out of DDR for Output DDR    | E, G                          | 0.259             | ns    |
| $t_{DDROSUDF}$   | DF Data Setup for Output DDR          | F, E                          | 0.28              | ns    |
| $t_{DDROSUDR}$   | DR Data Setup for Output DDR          | A, E                          | 0.289             | ns    |
| $t_{DDROHDF}$    | DF Data Hold for Output DDR           | F, E                          | 0.089             | ns    |
| $t_{DDROHDR}$    | DR Data Hold for Output DDR           | A, E                          | 0.078             | ns    |
| $t_{DDROSUE}$    | Enable Setup for Output DDR           | B, E                          | 0.832             | ns    |
| $t_{DDROHE}$     | Enable Hold for Output DDR            | B, E                          | 0.031             | ns    |
| $t_{DDROSUSL_n}$ | Synchronous Load Setup for Output DDR | D, E                          | 1.838             | ns    |
| $t_{DDROHSL_n}$  | Synchronous Load Hold for Output DDR  | D, E                          | 0.042             | ns    |

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**TABLE 2-85: OUTPUT DDR PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

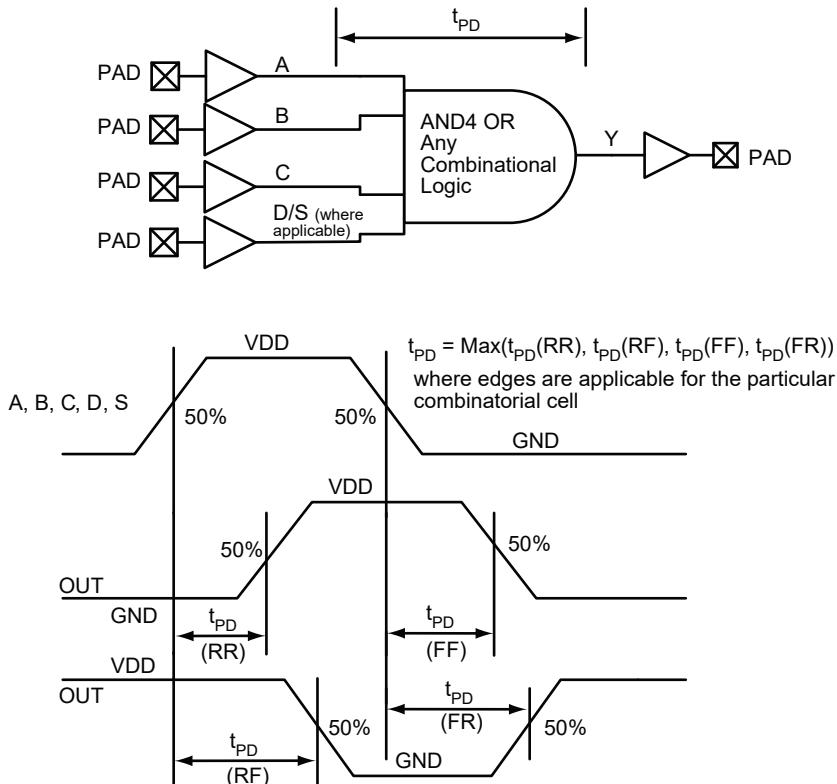
|                  |  |      |       |    |
|------------------|--|------|-------|----|
| $t_{DDROAL2Q}$   | Asynchronous Load-to-Out for Output DDR              | C, G | 0.552 | ns |
| $t_{DDROREMAL}$  | Asynchronous Load Removal time for Output DDR        | C, E | 0.135 | ns |
| $t_{DDRORECAL}$  | Asynchronous Load Recovery time for Output DDR       | C, E | 0.239 | ns |
| $t_{DDROWAL}$    | Asynchronous Load Minimum Pulse Width for Output DDR | C, C | 0.377 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR    | E, E | 0.101 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR     | E, E | 0.223 | ns |

## 3.0 LOGIC ELEMENT SPECIFICATIONS

### 3.1 4-input LUT (LUT-4)

The IGLOO 2 FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see the [SmartFusion2 and IGLOO2 Macro Library Guide](#).

**FIGURE 3-1: LUT-4**



#### 3.1.1 TIMING CHARACTERISTICS

The following table lists the combinational cell propagation delays.

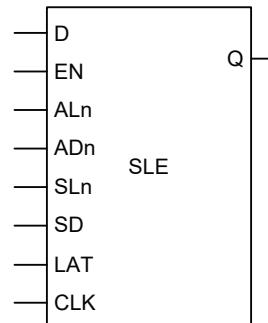
**TABLE 3-1: COMBINATORIAL CELL PROPAGATION DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Combinatorial Cell | Equation                        | Parameter | Speed Grade<br>-1 | Units |
|--------------------|---------------------------------|-----------|-------------------|-------|
| INV                | $Y = !A$                        | $t_{PD}$  | 0.104             | ns    |
| AND2               | $Y = A \cdot B$                 | $t_{PD}$  | 0.17              | ns    |
| NAND2              | $Y = !(A \cdot B)$              | $t_{PD}$  | 0.153             | ns    |
| OR2                | $Y = A + B$                     | $t_{PD}$  | 0.17              | ns    |
| NOR2               | $Y = !(A + B)$                  | $t_{PD}$  | 0.153             | ns    |
| XOR2               | $Y = A \oplus B$                | $t_{PD}$  | 0.17              | ns    |
| XOR3               | $Y = A \oplus B \oplus C$       | $t_{PD}$  | 0.234             | ns    |
| AND3               | $Y = A \cdot B \cdot C$         | $t_{PD}$  | 0.218             | ns    |
| AND4               | $Y = A \cdot B \cdot C \cdot D$ | $t_{PD}$  | 0.299             | ns    |

## 3.2 Sequential Module

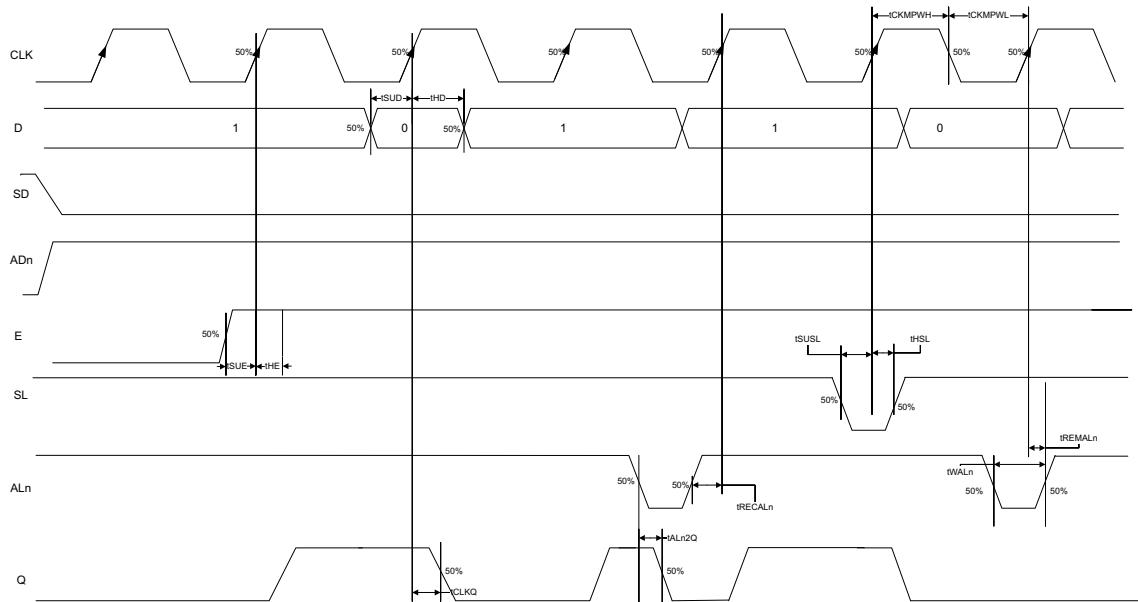
IGLOO 2 FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset). The following figure shows the sequential module.

**FIGURE 3-2: SEQUENTIAL MODULE**



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

**FIGURE 3-3: SEQUENTIAL MODULE TIMING DIAGRAM**



### 3.2.1 TIMING CHARACTERISTICS

The following table lists the register delays.

**TABLE 3-2: REGISTER DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $V_{DD} = 1.14\text{V}$**

| Parameter  | Description                     | Speed Grade -1 | Units |
|------------|---------------------------------|----------------|-------|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.114          | ns    |

**TABLE 3-2: REGISTER DELAYS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^{\circ}\text{C}$ ,  $VDD = 1.14\text{V}$**

|              |   |       |    |
|--------------|---|-------|----|
| $t_{SUD}$    | Data Setup Time for the Core Register                       | 0.263 | ns |
| $t_{HD}$     | Data Hold Time for the Core Register                        | 0     | ns |
| $t_{SUE}$    | Enable Setup Time for the Core Register                     | 0.319 | ns |
| $t_{HE}$     | Enable Hold Time for the Core Register                      | 0     | ns |
| $t_{SUSL}$   | Synchronous Load Setup Time for the Core Register           | 0.568 | ns |
| $t_{HSL}$    | Synchronous Load Hold Time for the Core Register            | 0     | ns |
| $t_{ALn2Q}$  | Asynchronous Clear-to-Q of the Core Register ( $ADn=1$ )    | 0.497 | ns |
|              | Asynchronous Preset-to-Q of the Core Register ( $ADn=0$ )   | 0.472 | ns |
| $t_{REMALn}$ | Asynchronous Load Removal Time for the Core Register        | 0     | ns |
| $t_{RECALn}$ | Asynchronous Load Recovery Time for the Core Register       | 0.367 | ns |
| $t_{WALn}$   | Asynchronous Load Minimum Pulse Width for the Core Register | 0.266 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register        | 0.065 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register         | 0.139 | ns |

## 4.0 GLOBAL RESOURCE CHARACTERISTICS

The IGLOO 2 FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. For the positions of various global routing resources, see the [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#).

The following tables lists the global resource characteristics.

**TABLE 4-1: M2GL090 DEVICE GLOBAL RESOURCE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter   | Description                       | Speed Grade -1 |       | Units |
|-------------|-----------------------------------|----------------|-------|-------|
|             |                                   | Min            | Max   |       |
| $t_{RCKL}$  | Input Low Delay for Global Clock  | 0.918          | 0.98  | ns    |
| $t_{RCKH}$  | Input High Delay for Global Clock | 1.702          | 1.815 | ns    |
| $t_{RCKSW}$ | Maximum Skew for Global Clock     | —              | 0.113 | ns    |

**TABLE 4-2: M2GL060 DEVICE GLOBAL RESOURCE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter   | Description                       | Speed Grade -1 |       | Units |
|-------------|-----------------------------------|----------------|-------|-------|
|             |                                   | Min            | Max   |       |
| $t_{RCKL}$  | Input Low Delay for Global Clock  | 1.031          | 1.08  | ns    |
| $t_{RCKH}$  | Input High Delay for Global Clock | 1.833          | 1.915 | ns    |
| $t_{RCKSW}$ | Maximum Skew for Global Clock     | —              | 0.082 | ns    |

**TABLE 4-3: M2GL025 DEVICE GLOBAL RESOURCE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter   | Description                       | Speed Grade -1 |       | Units |
|-------------|-----------------------------------|----------------|-------|-------|
|             |                                   | Min            | Max   |       |
| $t_{RCKL}$  | Input Low Delay for Global Clock  | 0.791          | 0.847 | ns    |
| $t_{RCKH}$  | Input High Delay for Global Clock | 1.41           | 1.506 | ns    |
| $t_{RCKSW}$ | Maximum Skew for Global Clock     | —              | 0.096 | ns    |

**TABLE 4-4: M2GL010 DEVICE GLOBAL RESOURCE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter   | Description                       | Speed Grade -1 |       | Units |
|-------------|-----------------------------------|----------------|-------|-------|
|             |                                   | Min            | Max   |       |
| $t_{RCKL}$  | Input Low Delay for Global Clock  | 0.61           | 0.66  | ns    |
| $t_{RCKH}$  | Input High Delay for Global Clock | 1.114          | 1.209 | ns    |
| $t_{RCKSW}$ | Maximum Skew for Global Clock     | —              | 0.095 | ns    |

**TABLE 4-5: M2GL005 DEVICE GLOBAL RESOURCE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter | Description | Speed Grade -1 |     | Units |
|-----------|-------------|----------------|-----|-------|
|           |             | Min            | Max |       |
|           |             |                |     |       |

---

**TABLE 4-5: M2GL005 DEVICE GLOBAL RESOURCE—WORST-CASE AUTOMOTIVE GRADE 1  
CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

|             |                                   |       |       |    |
|-------------|-----------------------------------|-------|-------|----|
| $t_{RCKL}$  | Input Low Delay for Global Clock  | 0.736 | 0.789 | ns |
| $t_{RCKH}$  | Input High Delay for Global Clock | 0.927 | 0.995 | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock     | —     | 0.068 | ns |

## 5.0 FPGA FABRIC SRAM

For more information, see the [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#).

### 5.1 FPGA Fabric Large SRAM (LSRAM)

The following tables list the parameters for the various RAM1K18 configurations.

**TABLE 5-1: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 1KX18—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter       | Description  | Speed Grade<br>-1 |       | Units |
|-----------------|--|-------------------|-------|-------|
|                 |  | Min               | Max   |       |
| $t_{CY}$        | Clock Period   | 3.333             | —     | ns    |
| $t_{CLKMPWH}$   | Clock Minimum Pulse Width High   | 1.5               | —     | ns    |
| $t_{CLKMPWL}$   | Clock Minimum pulse Width Low  | 1.5               | —     | ns    |
| $t_{PLCY}$      | Pipelined Clock Period   | 3.333             | —     | ns    |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High                                     | 1.5               | —     | ns    |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low                                      | 1.5               | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register                                      | —                 | 0.348 | ns    |
|                 | Read Access Time without Pipeline Register                                   | —                 | 2.355 | ns    |
|                 | Access Time with Feed-Through Write Timing                                   | —                 | 2.355 | ns    |
| $t_{ADDRSU}$    | Address Setup Time   | 0.457             | —     | ns    |
| $t_{ADDRHD}$    | Address Hold Time  | 0.284             | —     | ns    |
| $t_{DSU}$       | Data Setup Time  | 0.353             | —     | ns    |
| $t_{DHD}$       | Data Hold Time   | 0.111             | —     | ns    |
| $t_{BLKSU}$     | Block Select Setup Time  | 0.215             | —     | ns    |
| $t_{BLKHD}$     | Block Select Hold Time   | 0.224             | —     | ns    |
| $t_{BLK2Q}$     | Block Select to Out Disable Time<br>(when Pipe-Lined Registered is Disabled) | —                 | 1.584 | ns    |
| $t_{BLKMPW}$    | Block Select Minimum Pulse Width   | 0.218             | —     | ns    |
| $t_{RDESU}$     | Read Enable Setup Time   | 0.465             | —     | ns    |
| $t_{RDEHD}$     | Read Enable Hold Time  | 0.174             | —     | ns    |
| $t_{RDPLESU}$   | Pipelined Read Enable Setup Time<br>(A_DOUT_EN, B_DOUT_EN)                   | 0.257             | —     | ns    |
| $t_{RDPLEHD}$   | Pipelined Read Enable Hold Time<br>(A_DOUT_EN, B_DOUT_EN)                    | 0.106             | —     | ns    |
| $t_{R2Q}$       | Asynchronous Reset to Output Propagation Delay                               | —                 | 1.567 | ns    |
| $t_{RSTREM}$    | Asynchronous Reset Removal Time  | 0.524             | —     | ns    |
| $t_{RSTREC}$    | Asynchronous Reset Recovery Time   | 0.005             | —     | ns    |
| $t_{RSTMPW}$    | Asynchronous Reset Minimum Pulse Width                                       | 0.352             | —     | ns    |
| $t_{PLRSTREM}$  | Pipelined Register Asynchronous Reset Removal Time                           | -0.289            | —     | ns    |
| $t_{PLRSTREC}$  | Pipelined Register Asynchronous Reset Recovery Time                          | 0.339             | —     | ns    |
| $t_{PLRSTMPW}$  | Pipelined Register Asynchronous Reset Minimum Pulse Width                    | 0.33              | —     | ns    |
| $t_{SRSTSU}$    | Synchronous Reset Setup Time   | 0.234             | —     | ns    |
| $t_{SRSTHD}$    | Synchronous Reset Hold Time  | 0.038             | —     | ns    |
| $t_{WESU}$      | Write Enable Setup Time  | 0.404             | —     | ns    |
| $t_{WEHD}$      | Write Enable Hold Time   | 0.251             | —     | ns    |

**TABLE 5-1: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 1KX18—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter | Description       | Speed Grade -1 |     | Units |
|-----------|-------------------|----------------|-----|-------|
|           |                   | Min            | Max |       |
| Fmax      | Maximum Frequency | —              | 300 | MHz   |

**TABLE 5-2: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 2KX9—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description  | Speed Grade -1 |       | Units |
|-----------------|--|----------------|-------|-------|
|                 |  | Min            | Max   |       |
| $t_{CY}$        | Clock Period   | 3.333          | —     | ns    |
| $t_{CLKMPWH}$   | Clock Minimum Pulse Width High   | 1.5            | —     | ns    |
| $t_{CLKMPWL}$   | Clock Minimum pulse Width Low  | 1.5            | —     | ns    |
| $t_{PLCY}$      | Pipelined Clock Period   | 3.333          | —     | ns    |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High                                     | 1.5            | —     | ns    |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low                                      | 1.5            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register                                      | —              | 0.348 | ns    |
|                 | Read Access Time without Pipeline Register                                   | —              | 2.355 | ns    |
|                 | Access Time with Feed-Through Write Timing                                   | —              | 2.355 | ns    |
| $t_{ADDRSU}$    | Address Setup Time   | 0.492          | —     | ns    |
| $t_{ADDRHD}$    | Address Hold Time  | 0.284          | —     | ns    |
| $t_{DSU}$       | Data Setup Time  | 0.348          | —     | ns    |
| $t_{DHD}$       | Data Hold Time   | 0.084          | —     | ns    |
| $t_{BLKSU}$     | Block Select Setup Time  | 0.215          | —     | ns    |
| $t_{BLKHD}$     | Block Select Hold Time   | 0.224          | —     | ns    |
| $t_{BLK2Q}$     | Block Select to Out Disable Time<br>(when Pipe-Lined Registered is Disabled) | —              | 1.585 | ns    |
| $t_{BLKMPW}$    | Block Select Minimum Pulse Width   | 0.218          | —     | ns    |
| $t_{RDESU}$     | Read Enable Setup Time   | 0.502          | —     | ns    |
| $t_{RDEHD}$     | Read Enable Hold Time  | 0.073          | —     | ns    |
| $t_{RDPLESU}$   | Pipelined Read Enable Setup Time<br>(A_DOUT_EN, B_DOUT_EN)                   | 0.257          | —     | ns    |
| $t_{RDPLEHD}$   | Pipelined Read Enable Hold Time<br>(A_DOUT_EN, B_DOUT_EN)                    | 0.106          | —     | ns    |
| $t_{R2Q}$       | Asynchronous Reset to Output Propagation Delay                               | —              | 1.575 | ns    |
| $t_{RSTREM}$    | Asynchronous Reset Removal Time  | 0.524          | —     | ns    |
| $t_{RSTREC}$    | Asynchronous Reset Recovery Time   | 0.005          | —     | ns    |
| $t_{RSTMPW}$    | Asynchronous Reset Minimum Pulse Width                                       | 0.352          | —     | ns    |
| $t_{PLRSTREM}$  | Pipelined Register Asynchronous Reset Removal Time                           | -0.289         | —     | ns    |
| $t_{PLRSTREC}$  | Pipelined Register Asynchronous Reset Recovery Time                          | 0.339          | —     | ns    |
| $t_{PLRSTMPW}$  | Pipelined Register Asynchronous Reset Minimum Pulse Width                    | 0.33           | —     | ns    |
| $t_{SRSTSU}$    | Synchronous Reset Setup Time   | 0.234          | —     | ns    |
| $t_{SRSTHD}$    | Synchronous Reset Hold Time  | 0.038          | —     | ns    |

**TABLE 5-2: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 2KX9—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter  | Description             | Speed Grade -1 |     | Units |
|------------|-------------------------|----------------|-----|-------|
|            |                         | Min            | Max |       |
| $t_{WESU}$ | Write Enable Setup Time | 0.43           | —   | ns    |
| $t_{WEHD}$ | Write Enable Hold Time  | 0.05           | —   | ns    |
| Fmax       | Maximum Frequency       | —              | 300 | MHz   |

**TABLE 5-3: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 4KX4—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description   | Speed Grade -1 |       |       |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   | Units |
| $t_{CY}$        | Clock Period  | 3.333          | —     | ns    |
| $t_{CLKMPWH}$   | Clock Minimum Pulse Width High  | 1.5            | —     | ns    |
| $t_{CLKMPWL}$   | Clock Minimum pulse Width Low   | 1.5            | —     | ns    |
| $t_{PLCY}$      | Pipelined Clock Period  | 3.333          | —     | ns    |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High                                  | 1.5            | —     | ns    |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low                                   | 1.5            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register                                   | —              | 0.336 | ns    |
|                 | Read Access Time without Pipeline Register                                | —              | 2.355 | ns    |
|                 | Access Time with Feed-Through Write Timing                                | —              | 2.355 | ns    |
| $t_{ADDRSU}$    | Address Setup Time  | 0.562          | —     | ns    |
| $t_{ADDRHD}$    | Address Hold Time   | 0.284          | —     | ns    |
| $t_{DSU}$       | Data Setup Time   | 0.346          | —     | ns    |
| $t_{DHD}$       | Data Hold Time  | 0.084          | —     | ns    |
| $t_{BLKSU}$     | Block Select Setup Time   | 0.215          | —     | ns    |
| $t_{BLKHD}$     | Block Select Hold Time  | 0.224          | —     | ns    |
| $t_{BLK2Q}$     | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | —              | 1.566 | ns    |
| $t_{BLKMPW}$    | Block Select Minimum Pulse Width  | 0.218          | —     | ns    |
| $t_{RDESU}$     | Read Enable Setup Time  | 0.535          | —     | ns    |
| $t_{RDEHD}$     | Read Enable Hold Time   | 0.073          | —     | ns    |
| $t_{RDPLESU}$   | Pipelined Read Enable Setup Time (A_DOUT_EN, B_D-OUT_EN)                  | 0.257          | —     | ns    |
| $t_{RDPLEHD}$   | Pipelined Read Enable Hold Time (A_DOUT_EN, B_D-OUT_EN)                   | 0.106          | —     | ns    |
| $t_{R2Q}$       | Asynchronous Reset to Output Propagation Delay                            | —              | 1.568 | ns    |
| $t_{RSTREM}$    | Asynchronous Reset Removal Time   | 0.524          | —     | ns    |
| $t_{RSTREC}$    | Asynchronous Reset Recovery Time  | 0.005          | —     | ns    |
| $t_{RSTMPW}$    | Asynchronous Reset Minimum Pulse Width                                    | 0.352          | —     | ns    |
| $t_{PLRSTREM}$  | Pipelined Register Asynchronous Reset Removal Time                        | -0.289         | —     | ns    |
| $t_{PLRSTREC}$  | Pipelined Register Asynchronous Reset Recovery Time                       | 0.339          | —     | ns    |
| $t_{PLRSTMPW}$  | Pipelined Register Asynchronous Reset Minimum Pulse Width                 | 0.33           | —     | ns    |
| $t_{SRSTSU}$    | Synchronous Reset Setup Time  | 0.234          | —     | ns    |

**TABLE 5-3: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 4KX4—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter    | Description                 | Speed Grade -1 |     |       |
|--------------|-----------------------------|----------------|-----|-------|
|              |                             | Min            | Max | Units |
| $t_{SRSTHD}$ | Synchronous Reset Hold Time | 0.038          | —   | ns    |
| $t_{WESU}$   | Write Enable Setup Time     | 0.475          | —   | ns    |
| $t_{WEHD}$   | Write Enable Hold Time      | 0.05           | —   | ns    |
| Fmax         | Maximum Frequency           | —              | 300 | MHz   |

**TABLE 5-4: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 8KX2—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description  | Speed Grade -1 |       | Units |
|-----------------|--|----------------|-------|-------|
|                 |  | Min            | Max   |       |
| $t_{CY}$        | Clock Period   | 3.333          | —     | ns    |
| $t_{CLKMPWH}$   | Clock Minimum Pulse Width High   | 1.5            | —     | ns    |
| $t_{CLKMPWL}$   | Clock Minimum pulse Width Low  | 1.5            | —     | ns    |
| $t_{PLCY}$      | Pipelined Clock Period   | 3.333          | —     | ns    |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High                                     | 1.5            | —     | ns    |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low                                      | 1.5            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register                                      | —              | 0333  | ns    |
|                 | Read Access Time without Pipeline Register                                   | —              | 2.355 | ns    |
|                 | Access Time with Feed-Through Write Timing                                   | —              | 2.355 | ns    |
| $t_{ADDRSU}$    | Address Setup Time   | 0.634          | —     | ns    |
| $t_{ADDRHD}$    | Address Hold Time  | 0.284          | —     | ns    |
| $t_{DSU}$       | Data Setup Time  | 0.342          | —     | ns    |
| $t_{DHD}$       | Data Hold Time   | 0.084          | —     | ns    |
| $t_{BLKSU}$     | Block Select Setup Time  | 0.215          | —     | ns    |
| $t_{BLKHD}$     | Block Select Hold Time   | 0.224          | —     | ns    |
| $t_{BLK2Q}$     | Block Select to Out Disable Time<br>(when Pipe-Lined Registered is Disabled) | —              | 1.566 | ns    |
| $t_{BLKMPW}$    | Block Select Minimum Pulse Width   | 0.218          | —     | ns    |
| $t_{RDESU}$     | Read Enable Setup Time   | 0.548          | —     | ns    |
| $t_{RDEHD}$     | Read Enable Hold Time  | 0.073          | —     | ns    |
| $t_{RDPLESU}$   | Pipelined Read Enable Setup Time<br>(A_DOUT_EN, B_DOUT_EN)                   | 0.257          | —     | ns    |
| $t_{RDPLEHD}$   | Pipelined Read Enable Hold Time<br>(A_DOUT_EN, B_DOUT_EN)                    | 0.106          | —     | ns    |
| $t_{R2Q}$       | Asynchronous Reset to Output Propagation Delay                               | —              | 1.59  | ns    |
| $t_{RSTREM}$    | Asynchronous Reset Removal Time  | 0.524          | —     | ns    |
| $t_{RSTREC}$    | Asynchronous Reset Recovery Time   | 0.005          | —     | ns    |
| $t_{RSTMPW}$    | Asynchronous Reset Minimum Pulse Width                                       | 0.352          | —     | ns    |
| $t_{PLRSTREM}$  | Pipelined Register Asynchronous Reset Removal Time                           | -0.289         | —     | ns    |
| $t_{PLRSTREC}$  | Pipelined Register Asynchronous Reset Recovery Time                          | 0.339          | —     | ns    |
| $t_{PLRSTMPW}$  | Pipelined Register Asynchronous Reset Minimum Pulse Width                    | 0.33           | —     | ns    |

**TABLE 5-4: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 8KX2—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter    | Description                  | Speed Grade -1 |     | Units |
|--------------|------------------------------|----------------|-----|-------|
|              |                              | Min            | Max |       |
| $t_{SRSTSU}$ | Synchronous Reset Setup Time | 0.234          | —   | ns    |
| $t_{SRSTHD}$ | Synchronous Reset Hold Time  | 0.038          | —   | ns    |
| $t_{WESU}$   | Write Enable Setup Time      | 0.506          | —   | ns    |
| $t_{WEHD}$   | Write Enable Hold Time       | 0.05           | —   | ns    |
| Fmax         | Maximum Frequency            | —              | 300 | MHz   |

**TABLE 5-5: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 16KX1—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description   | Speed Grade -1 |       | Units |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   |       |
| $t_{CY}$        | Clock Period  | 3.333          | —     | ns    |
| $t_{CLKMPWH}$   | Clock Minimum Pulse Width High  | 1.5            | —     | ns    |
| $t_{CLKMPWL}$   | Clock Minimum pulse Width Low   | 1.5            | —     | ns    |
| $t_{PLCY}$      | Pipelined Clock Period  | 3.333          | —     | ns    |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High                                  | 1.5            | —     | ns    |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low                                   | 1.5            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register                                   | —              | 0.333 | ns    |
|                 | Read Access Time without Pipeline Register                                | —              | 2.351 | ns    |
|                 | Access Time with Feed-Through Write Timing                                | —              | 2.351 | ns    |
| $t_{ADDRSU}$    | Address Setup Time  | 0.649          | —     | ns    |
| $t_{ADDRHD}$    | Address Hold Time   | 0.284          | —     | ns    |
| $t_{DSU}$       | Data Setup Time   | 0.333          | —     | ns    |
| $t_{DHD}$       | Data Hold Time  | 0.084          | —     | ns    |
| $t_{BLKSU}$     | Block Select Setup Time   | 0.215          | —     | ns    |
| $t_{BLKHD}$     | Block Select Hold Time  | 0.224          | —     | ns    |
| $t_{BLK2Q}$     | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | —              | 1.565 | ns    |
| $t_{BLKMPW}$    | Block Select Minimum Pulse Width  | 0.218          | —     | ns    |
| $t_{RDESU}$     | Read Enable Setup Time  | 0.549          | —     | ns    |
| $t_{RDEHD}$     | Read Enable Hold Time   | 0.073          | —     | ns    |
| $t_{RDPLESU}$   | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)                   | 0.257          | —     | ns    |
| $t_{RDPLEHD}$   | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)                    | 0.106          | —     | ns    |
| $t_{R2Q}$       | Asynchronous Reset to Output Propagation Delay                            | —              | 1.609 | ns    |
| $t_{RSTREM}$    | Asynchronous Reset Removal Time   | 0.524          | —     | ns    |
| $t_{RSTREC}$    | Asynchronous Reset Recovery Time  | 0.005          | —     | ns    |
| $t_{RSTMPW}$    | Asynchronous Reset Minimum Pulse Width                                    | 0.352          | —     | ns    |
| $t_{PLRSTREM}$  | Pipelined Register Asynchronous Reset Removal Time                        | -0.289         | —     | ns    |
| $t_{PLRSTREC}$  | Pipelined Register Asynchronous Reset Recovery Time                       | 0.339          | —     | ns    |
| $t_{PLRSTMPW}$  | Pipelined Register Asynchronous Reset Minimum Pulse Width                 | 0.33           | —     | ns    |
| $t_{SRSTSU}$    | Synchronous Reset Setup Time  | 0.234          | —     | ns    |

**TABLE 5-5: RAM1K18 – DUAL-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 16KX1—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter    | Description                 | Speed Grade -1 |     | Units |
|--------------|-----------------------------|----------------|-----|-------|
|              |                             | Min            | Max |       |
| $t_{SRSTHD}$ | Synchronous Reset Hold Time | 0.038          | —   | ns    |
| $t_{WESU}$   | Write Enable Setup Time     | 0.47           | —   | ns    |
| $t_{WEHD}$   | Write Enable Hold Time      | 0.05           | —   | ns    |
| Fmax         | Maximum Frequency           | —              | 300 | MHz   |

**TABLE 5-6: RAM1K18 – TWO-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 512X36—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description   | Speed Grade -1 |       | Units |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   |       |
| $t_{CY}$        | Clock Period  | 3.333          | —     | ns    |
| $t_{CLKMPWH}$   | Clock Minimum Pulse Width High  | 1.5            | —     | ns    |
| $t_{CLKMPWL}$   | Clock Minimum pulse Width Low   | 1.5            | —     | ns    |
| $t_{PLCY}$      | Pipelined Clock Period  | 3.333          | —     | ns    |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High                                  | 1.5            | —     | ns    |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low                                   | 1.5            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register                                   | —              | 0.347 | ns    |
|                 | Read Access Time without Pipeline Register                                | —              | 2.331 | ns    |
| $t_{ADDRSU}$    | Address Setup Time  | 0.324          | —     | ns    |
| $t_{ADDRHD}$    | Address Hold Time   | 0.284          | —     | ns    |
| $t_{DSU}$       | Data Setup Time   | 0.349          | —     | ns    |
| $t_{DHD}$       | Data Hold Time  | 0.115          | —     | ns    |
| $t_{BLKSU}$     | Block Select Setup Time   | 0.215          | —     | ns    |
| $t_{BLKHD}$     | Block Select Hold Time  | 0.209          | —     | ns    |
| $t_{BLK2Q}$     | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | —              | 2.331 | ns    |
| $t_{BLKMPW}$    | Block Select Minimum Pulse Width  | 0.218          | —     | ns    |
| $t_{RDESU}$     | Read Enable Setup Time  | 0.465          | —     | ns    |
| $t_{RDEHD}$     | Read Enable Hold Time   | 0.174          | —     | ns    |
| $t_{RDPLESU}$   | Pipelined Read Enable Setup Time (A_DOUT_EN, B_D-OUT_EN)                  | 0.257          | —     | ns    |
| $t_{RDPLEHD}$   | Pipelined Read Enable Hold Time (A_DOUT_EN, B_D-OUT_EN)                   | 0.106          | —     | ns    |
| $t_{R2Q}$       | Asynchronous Reset to Output Propagation Delay                            | —              | 1.567 | ns    |
| $t_{RSTREM}$    | Asynchronous Reset Removal Time   | 0.524          | —     | ns    |
| $t_{RSTREC}$    | Asynchronous Reset Recovery Time  | 0.005          | —     | ns    |
| $t_{RSTMPW}$    | Asynchronous Reset Minimum Pulse Width                                    | 0.352          | —     | ns    |
| $t_{PLRSTREM}$  | Pipelined Register Asynchronous Reset Removal Time                        | -0.289         | —     | ns    |
| $t_{PLRSTREC}$  | Pipelined Register Asynchronous Reset Recovery Time                       | 0.339          | —     | ns    |
| $t_{PLRSTMPW}$  | Pipelined Register Asynchronous Reset Minimum Pulse Width                 | 0.33           | —     | ns    |
| $t_{SRSTSU}$    | Synchronous Reset Setup Time  | 0.234          | —     | ns    |

**TABLE 5-6: RAM1K18 – TWO-PORT MODE FOR DEPTH × WIDTH CONFIGURATION 512X36—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter    | Description                 | Speed Grade -1 |     | Units |
|--------------|-----------------------------|----------------|-----|-------|
|              |                             | Min            | Max |       |
| $t_{SRSTHD}$ | Synchronous Reset Hold Time | 0.038          | —   | ns    |
| $t_{WESU}$   | Write Enable Setup Time     | 0.404          | —   | ns    |
| $t_{WEHD}$   | Write Enable Hold Time      | 0.251          | —   | ns    |
| Fmax         | Maximum Frequency           | —              | 300 | MHz   |

## 5.2 FPGA Fabric Micro SRAM (uSRAM)

The following tables list the parameters for the various modes of USRAM.

**TABLE 5-7: USRAM (RAM64X18) IN 64X18 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description  | Speed Grade -1 |       | Units |
|-----------------|--|----------------|-------|-------|
|                 |  | Min            | Max   |       |
| $t_{CY}$        | Read Clock Period  | 4              | —     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low   | 1.8            | —     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period  | 4              | —     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low   | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register  | —              | 0.277 | ns    |
|                 | Read Access Time without Pipeline Register   | —              | 1.745 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode  | 0.312          | —     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode   | 1.924          | —     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode   | 0.094          | —     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode  | -0.806         | —     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time   | 0.288          | —     | ns    |
| $t_{RDENHD}$    | Read Enable Hold Time  | 0.059          | —     | ns    |
| $t_{BLKSU}$     | Read Block Select Setup Time   | 1.905          | —     | ns    |
| $t_{BLKHD}$     | Read Block Select Hold Time  | -0.674         | —     | ns    |
| $t_{BLK2Q}$     | Read Block Select to Out Disable Time<br>(when Pipe-Lined Registered is Disabled)        | —              | 2.11  | ns    |
| $t_{RSTREM}$    | Read Asynchronous Reset Removal Time (Pipelined Clock)                                   | -0.151         | —     | ns    |
|                 | Read Asynchronous Reset Removal Time<br>(Non-Pipelined Clock)                            | 0.048          | —     | ns    |
| $t_{RSTREC}$    | Read Asynchronous Reset Recovery Time (Pipelined Clock)                                  | 0.526          | —     | ns    |
|                 | Read Asynchronous Reset Recovery Time<br>(Non-Pipelined Clock)                           | 0.245          | —     | ns    |
| $t_{R2Q}$       | Read Asynchronous Reset to Output Propagation Delay<br>(with Pipe-Line Register Enabled) | —              | 0.873 | ns    |
| $t_{SRSTSU}$    | Read Synchronous Reset Setup Time  | 0.281          | —     | ns    |
| $t_{SRSTHD}$    | Read Synchronous Reset Hold Time   | 0.063          | —     | ns    |
| $t_{CCY}$       | Write Clock Period   | 4              | —     | ns    |

**TABLE 5-7: USRAM (RAM64X18) IN 64X18 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V (CONTINUED)**

| Parameter      | Description                          | Speed Grade -1 |     | Units |
|----------------|--------------------------------------|----------------|-----|-------|
|                |                                      | Min            | Max |       |
| $t_{CCLKMPWH}$ | Write Clock Minimum Pulse Width High | 1.8            | —   | ns    |
| $t_{CCLKMPWL}$ | Write Clock Minimum Pulse Width Low  | 1.8            | —   | ns    |
| $t_{BLKCSU}$   | Write Block Setup Time               | 0.419          | —   | ns    |
| $t_{BLKCHD}$   | Write Block Hold Time                | 0.007          | —   | ns    |
| $t_{DINCSU}$   | Write Input Data setup Time          | 0.119          | —   | ns    |
| $t_{DINCHD}$   | Write Input Data hold Time           | 0.156          | —   | ns    |
| $t_{ADDRCSU}$  | Write Address Setup Time             | 0.091          | —   | ns    |
| $t_{ADDRCHD}$  | Write Address Hold Time              | 0.132          | —   | ns    |
| $t_{WECSU}$    | Write Enable Setup Time              | 0.412          | —   | ns    |
| $t_{WECHD}$    | Write Enable Hold Time               | -0.027         | —   | ns    |
| Fmax           | Maximum Frequency                    | —              | 250 | MHz   |

**TABLE 5-8: USRAM (RAM64X16) IN 64X16 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter       | Description  | Speed Grade -1 |       | Units |
|-----------------|--|----------------|-------|-------|
|                 |  | Min            | Max   |       |
| $t_{CY}$        | Read Clock Period  | 4              | —     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low   | 1.8            | —     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period  | 4              | —     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High                                  | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low                                   | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register  | —              | 0.277 | ns    |
|                 | Read Access Time without Pipeline Register                                     | —              | 1.745 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode                                    | 0.312          | —     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode                                   | 1.924          | —     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode                                     | 0.094          | —     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode                                    | -0.806         | —     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time   | 0.288          | —     | ns    |
| $t_{RDENHD}$    | Read Enable Hold Time  | 0.059          | —     | ns    |
| $t_{BLKSU}$     | Read Block Select Setup Time   | 1.905          | —     | ns    |
| $t_{BLKHD}$     | Read Block Select Hold Time  | -0.674         | —     | ns    |
| $t_{BLK2Q}$     | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | —              | 2.11  | ns    |
| $t_{RSTREM}$    | Read Asynchronous Reset Removal Time (Pipelined Clock)                         | -0.151         | —     | ns    |
|                 | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                     | 0.048          | —     | ns    |
| $t_{RSTREC}$    | Read Asynchronous Reset Recovery Time (Pipelined Clock)                        | 0.526          | —     | ns    |
|                 | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                    | 0.245          | —     | ns    |

**TABLE 5-8: USRAM (RAM64X16) IN 64X16 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

| Parameter      | Description   | Speed Grade -1 |       | Units |
|----------------|---|----------------|-------|-------|
|                |   | Min            | Max   |       |
| $t_{R2Q}$      | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | —              | 0.869 | ns    |
| $t_{SRSTSU}$   | Read Synchronous Reset Setup Time   | 0.281          | —     | ns    |
| $t_{SRSTHD}$   | Read Synchronous Reset Hold Time  | 0.063          | —     | ns    |
| $t_{CCY}$      | Write Clock Period  | 4              | —     | ns    |
| $t_{CCLKMPWH}$ | Write Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CCLKMPWL}$ | Write Clock Minimum Pulse Width Low   | 1.8            | —     | ns    |
| $t_{BLKCSU}$   | Write Block Setup Time  | 0.419          | —     | ns    |
| $t_{BLKCHD}$   | Write Block Hold Time   | 0.007          | —     | ns    |
| $t_{DINCSU}$   | Write Input Data setup Time   | 0.119          | —     | ns    |
| $t_{DINCHD}$   | Write Input Data hold Time  | 0.156          | —     | ns    |
| $t_{ADDRCSU}$  | Write Address Setup Time  | 0.091          | —     | ns    |
| $t_{ADDRCHD}$  | Write Address Hold Time   | 0.132          | —     | ns    |
| $t_{WECSU}$    | Write Enable Setup Time   | 0.412          | —     | ns    |
| $t_{WECHD}$    | Write Enable Hold Time  | -0.027         | —     | ns    |
| Fmax           | Maximum Frequency   | —              | 250   | MHz   |

**TABLE 5-9: USRAM (RAM128X9) IN 128X9 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter       | Description  | Speed Grade -1 |       | Units |
|-----------------|--|----------------|-------|-------|
|                 |  | Min            | Max   |       |
| $t_{CY}$        | Read Clock Period  | 4              | —     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low   | 1.8            | —     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period  | 4              | —     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High                                  | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low                                   | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register  | —              | 0.277 | ns    |
|                 | Read Access Time without Pipeline Register                                     | —              | 1.783 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode                                    | 0.312          | —     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode                                   | 1.967          | —     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode                                     | 0.125          | —     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode                                    | -0.707         | —     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time   | 0.288          | —     | ns    |
| $t_{RDENHD}$    | Read Enable Hold Time  | 0.059          | —     | ns    |
| $t_{BLKSU}$     | Read Block Select Setup Time   | 1.905          | —     | ns    |
| $t_{BLKHD}$     | Read Block Select Hold Time  | -0.674         | —     | ns    |
| $t_{BLK2Q}$     | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | —              | 2.148 | ns    |

**TABLE 5-9: USRAM (RAM128X9) IN 128X9 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

| Parameter      | Description   | Speed Grade -1 |       | Units |
|----------------|---|----------------|-------|-------|
|                |   | Min            | Max   |       |
| $t_{RSTREM}$   | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.151         | —     | ns    |
|                | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.048          | —     | ns    |
| $t_{RSTREC}$   | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.526          | —     | ns    |
|                | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.245          | —     | ns    |
| $t_{R2Q}$      | Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled) | —              | 0.869 | ns    |
| $t_{SRSTSU}$   | Read Synchronous Reset Setup Time   | 0.281          | —     | ns    |
| $t_{SRSTHD}$   | Read Synchronous Reset Hold Time  | 0.063          | —     | ns    |
| $t_{CCY}$      | Write Clock Period  | 4              | —     | ns    |
| $t_{CCLKMPWH}$ | Write Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CCLKMPWL}$ | Write Clock Minimum Pulse Width Low   | 1.8            | —     | ns    |
| $t_{BLKCSU}$   | Write Block Setup Time  | 0.419          | —     | ns    |
| $t_{BLKCHD}$   | Write Block Hold Time   | 0.007          | —     | ns    |
| $t_{DINCSU}$   | Write Input Data setup Time   | 0.104          | —     | ns    |
| $t_{DINCHD}$   | Write Input Data hold Time  | 0.142          | —     | ns    |
| $t_{ADDRCSU}$  | Write Address Setup Time  | 0.091          | —     | ns    |
| $t_{ADDRCHD}$  | Write Address Hold Time   | 0.241          | —     | ns    |
| $t_{WECSU}$    | Write Enable Setup Time   | 0.412          | —     | ns    |
| $t_{WECHD}$    | Write Enable Hold Time  | -0.027         | —     | ns    |
| Fmax           | Maximum Frequency   | —              | 250   | MHz   |

**TABLE 5-10: USRAM (RAM128X8) IN 128X8 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter       | Description                                   | Speed Grade -1 |       | Units |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   |       |
| $t_{CY}$        | Read Clock Period                             | 4              | —     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High           | 1.8            | —     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low            | 1.8            | —     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period                   | 4              | —     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low  | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register       | —              | 0.277 | ns    |
|                 | Read Access Time without Pipeline Register    | —              | 1.783 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode   | 0.312          | —     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode  | 1.967          | —     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode    | 0.125          | —     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode   | -0.707         | —     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time                        | 0.288          | —     | ns    |

**TABLE 5-10: USRAM (RAM128X8) IN 128X8 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

| Parameter      | Description   | Speed Grade -1 |       | Units |
|----------------|---|----------------|-------|-------|
|                |   | Min            | Max   |       |
| $t_{RDENHD}$   | Read Enable Hold Time   | 0.059          | —     | ns    |
| $t_{BLKSU}$    | Read Block Select Setup Time  | 1.905          | —     | ns    |
| $t_{BLKHD}$    | Read Block Select Hold Time   | -0.674         | —     | ns    |
| $t_{BLK2Q}$    | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)        | —              | 2.148 | ns    |
| $t_{RSTREM}$   | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.151         | —     | ns    |
|                | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.048          | —     | ns    |
| $t_{RSTREC}$   | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.526          | —     | ns    |
|                | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.245          | —     | ns    |
| $t_{R2Q}$      | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | —              | 0.869 | ns    |
| $t_{SRSTSU}$   | Read Synchronous Reset Setup Time   | 0.281          | —     | ns    |
| $t_{SRSTHD}$   | Read Synchronous Reset Hold Time  | 0.063          | —     | ns    |
| $t_{CCY}$      | Write Clock Period  | 4              | —     | ns    |
| $t_{CCLKMPWH}$ | Write Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CCLKMPWL}$ | Write Clock Minimum Pulse Width Low   | 1.8            | —     | ns    |
| $t_{BLKCSU}$   | Write Block Setup Time  | 0.419          | —     | ns    |
| $t_{BLKCHD}$   | Write Block Hold Time   | 0.007          | —     | ns    |
| $t_{DINCSU}$   | Write Input Data setup Time   | 0.104          | —     | ns    |
| $t_{DINCHD}$   | Write Input Data hold Time  | 0.142          | —     | ns    |
| $t_{ADDRCSU}$  | Write Address Setup Time  | 0.091          | —     | ns    |
| $t_{ADDRCHD}$  | Write Address Hold Time   | 0.241          | —     | ns    |
| $t_{WECSU}$    | Write Enable Setup Time   | 0.412          | —     | ns    |
| $t_{WECHD}$    | Write Enable Hold Time  | -0.027         | —     | ns    |
| Fmax           | Maximum Frequency   | —              | 250   | MHz   |

**TABLE 5-11: USRAM (RAM256X4) IN 256X4 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter       | Description                                   | Speed Grade -1 |       | Units |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   |       |
| $t_{CY}$        | Read Clock Period                             | 4              | —     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High           | 1.8            | —     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low            | 1.8            | —     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period                   | 4              | —     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low  | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register       | —              | 0.277 | ns    |
|                 | Read Access Time without Pipeline Register    | —              | 1.819 | ns    |

**TABLE 5-11: USRAM (RAM256X4) IN 256X4 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

| Parameter      | Description   | Speed Grade – 1 |       | Units |
|----------------|---|-----------------|-------|-------|
|                |   | Min             | Max   |       |
| $t_{ADDRSU}$   | Read Address Setup Time in Synchronous Mode   | 0.312           | —     | ns    |
|                | Read Address Setup Time in Asynchronous Mode  | 2.001           | —     | ns    |
| $t_{ADDRHD}$   | Read Address Hold Time in Synchronous Mode  | 0.125           | —     | ns    |
|                | Read Address Hold Time in Asynchronous Mode   | -0.672          | —     | ns    |
| $t_{RDENSU}$   | Read Enable Setup Time  | 0.288           | —     | ns    |
| $t_{RDENHD}$   | Read Enable Hold Time   | 0.059           | —     | ns    |
| $t_{BLKSU}$    | Read Block Select Setup Time  | 1.905           | —     | ns    |
| $t_{BLKHD}$    | Read Block Select Hold Time   | -0.674          | —     | ns    |
| $t_{BLK2Q}$    | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)        | —               | 2.175 | ns    |
| $t_{RSTREM}$   | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.151          | —     | ns    |
|                | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.048           | —     | ns    |
| $t_{RSTREC}$   | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.526           | —     | ns    |
|                | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.245           | —     | ns    |
| $t_{R2Q}$      | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | —               | 0.866 | ns    |
| $t_{SRSTSU}$   | Read Synchronous Reset Setup Time   | 0.281           | —     | ns    |
| $t_{SRSTHD}$   | Read Synchronous Reset Hold Time  | 0.063           | —     | ns    |
| $t_{CCY}$      | Write Clock Period  | 4               | —     | ns    |
| $t_{CCLKMPWH}$ | Write Clock Minimum Pulse Width High  | 1.8             | —     | ns    |
| $t_{CCLKMPWL}$ | Write Clock Minimum Pulse Width Low   | 1.8             | —     | ns    |
| $t_{BLKCSU}$   | Write Block Setup Time  | 0.419           | —     | ns    |
| $t_{BLKCHD}$   | Write Block Hold Time   | 0.007           | —     | ns    |
| $t_{DINCSU}$   | Write Input Data setup Time   | 0.104           | —     | ns    |
| $t_{DINCHD}$   | Write Input Data hold Time  | 0.142           | —     | ns    |
| $t_{ADDRCSU}$  | Write Address Setup Time  | 0.091           | —     | ns    |
| $t_{ADDRCHD}$  | Write Address Hold Time   | 0.254           | —     | ns    |
| $t_{WECSU}$    | Write Enable Setup Time   | 0.412           | —     | ns    |
| $t_{WECHD}$    | Write Enable Hold Time  | -0.027          | —     | ns    |
| Fmax           | Maximum Frequency   | —               | 250   | MHz   |

**TABLE 5-12: USRAM (RAM512X2) IN 512X2 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter     | Description                         | Speed Grade –1 |     | Units |
|---------------|-------------------------------------|----------------|-----|-------|
|               |                                     | Min            | Max |       |
| $t_{CY}$      | Read Clock Period                   | 4              | —   | ns    |
| $t_{CLKMPWH}$ | Read Clock Minimum Pulse Width High | 1.8            | —   | ns    |
| $t_{CLKMPWL}$ | Read Clock Minimum pulse Width Low  | 1.8            | —   | ns    |
| $t_{PLCY}$    | Read Pipe-line clock period         | 4              | —   | ns    |

**TABLE 5-12: USRAM (RAM512X2) IN 512X2 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

| Parameter       | Description   | Speed Grade -1 |       | Units |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   |       |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High   | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low  | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register   | —              | 0.277 | ns    |
|                 | Read Access Time without Pipeline Register  | —              | 1.831 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode   | 0.312          | —     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode  | 2.031          | —     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode  | 0.142          | —     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode   | -0.602         | —     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time  | 0.288          | —     | ns    |
| $t_{RDENHD}$    | Read Enable Hold Time   | 0.059          | —     | ns    |
| $t_{BLKSU}$     | Read Block Select Setup Time  | 1.905          | —     | ns    |
| $t_{BLKHD}$     | Read Block Select Hold Time   | -0.674         | —     | ns    |
| $t_{BLK2Q}$     | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)        | —              | 2.228 | ns    |
| $t_{RSTREM}$    | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.151         | —     | ns    |
|                 | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.048          | —     | ns    |
| $t_{RSTREC}$    | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.526          | —     | ns    |
|                 | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.245          | —     | ns    |
| $t_{R2Q}$       | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | —              | 0.865 | ns    |
| $t_{SRSTSU}$    | Read Synchronous Reset Setup Time   | 0.281          | —     | ns    |
| $t_{SRSTHD}$    | Read Synchronous Reset Hold Time  | 0.063          | —     | ns    |
| $t_{CCY}$       | Write Clock Period  | 4              | —     | ns    |
| $t_{CCLKMPWH}$  | Write Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CCLKMPWL}$  | Write Clock Minimum Pulse Width Low   | 1.8            | —     | ns    |
| $t_{BLKCSU}$    | Write Block Setup Time  | 0.419          | —     | ns    |
| $t_{BLKCHD}$    | Write Block Hold Time   | 0.007          | —     | ns    |
| $t_{DINCSU}$    | Write Input Data setup Time   | 0.104          | —     | ns    |
| $t_{DINCHD}$    | Write Input Data hold Time  | 0.142          | —     | ns    |
| $t_{ADDRCSU}$   | Write Address Setup Time  | 0.091          | —     | ns    |
| $t_{ADDRCHD}$   | Write Address Hold Time   | 0.256          | —     | ns    |
| $t_{WECSU}$     | Write Enable Setup Time   | 0.412          | —     | ns    |
| $t_{WECHD}$     | Write Enable Hold Time  | -0.027         | —     | ns    |
| Fmax            | Maximum Frequency   | —              | 250   | MHz   |

**TABLE 5-13: USRAM (RAM1024X1) IN 1024X1 MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter       | Description   | Speed Grade -1 |       | Units |
|-----------------|---|----------------|-------|-------|
|                 |   | Min            | Max   |       |
| $t_{CY}$        | Read Clock Period   | 4              | —     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High   | 1.8            | —     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low  | 1.8            | —     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period   | 4              | —     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High   | 1.8            | —     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low  | 1.8            | —     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register   | —              | 0.275 | ns    |
|                 | Read Access Time without Pipeline Register  | —              | 1.846 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode   | 0.312          | —     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode  | 2.05           | —     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode  | 0.142          | —     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode   | -0.626         | —     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time  | 0.288          | —     | ns    |
| $t_{RDENHD}$    | Read Enable Hold Time   | 0.059          | —     | ns    |
| $t_{BLKSU}$     | Read Block Select Setup Time  | 1.905          | —     | ns    |
| $t_{BLKHD}$     | Read Block Select Hold Time   | -0.674         | —     | ns    |
| $t_{BLK2Q}$     | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)        | —              | 2.245 | ns    |
| $t_{RSTREM}$    | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.151         | —     | ns    |
|                 | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.048          | —     | ns    |
| $t_{RSTREC}$    | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.526          | —     | ns    |
|                 | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.245          | —     | ns    |
| $t_{R2Q}$       | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | —              | 0.865 | ns    |
| $t_{SRSTSU}$    | Read Synchronous Reset Setup Time   | 0.281          | —     | ns    |
| $t_{SRSTHD}$    | Read Synchronous Reset Hold Time  | 0.063          | —     | ns    |
| $t_{CCY}$       | Write Clock Period  | 4              | —     | ns    |
| $t_{CCLKMPWH}$  | Write Clock Minimum Pulse Width High  | 1.8            | —     | ns    |
| $t_{CCLKMPWL}$  | Write Clock Minimum Pulse Width Low   | 1.8            | —     | ns    |
| $t_{BLKCSU}$    | Write Block Setup Time  | 0.419          | —     | ns    |
| $t_{BLKCHD}$    | Write Block Hold Time   | 0.007          | —     | ns    |
| $t_{DINCSU}$    | Write Input Data setup Time   | 0.003          | —     | ns    |
| $t_{DINCHD}$    | Write Input Data hold Time  | 0.142          | —     | ns    |
| $t_{ADDRCSU}$   | Write Address Setup Time  | 0.091          | —     | ns    |
| $t_{ADDRCHD}$   | Write Address Hold Time   | 0.256          | —     | ns    |
| $t_{WECSU}$     | Write Enable Setup Time   | 0.412          | —     | ns    |
| $t_{WECHD}$     | Write Enable Hold Time  | -0.027         | —     | ns    |
| Fmax            | Maximum Frequency   | —              | 250   | MHz   |

## 6.0 SWITCHING CHARACTERISTICS

### 6.1 Embedded NVM (eNVM) Characteristics

The following tables list the ENVM characteristics.

**TABLE 6-1: ENVN READ PERFORMANCE—WORST-CASE CONDITIONS: VDD = 1.14V, VPPNVM = VPP = 2.375V**

| Symbol               | Description                 | Operating Temperature Range |   | Unit |
|----------------------|-----------------------------|-----------------------------|---|------|
| T <sub>J</sub>       | Junction Temperature Range  | −40 °C to 135 °C            |   | °C   |
| Speed grade          | —                           | −1                          | — | —    |
| F <sub>MAXREAD</sub> | eNVM Maximum Read Frequency | 25                          | — | MHz  |

**TABLE 6-2: ENVN PAGE PROGRAMMING—WORST-CASE CONDITIONS: VDD = 1.14V, VPPNVM = VPP = 2.375V**

| Symbol               | Description                | Operating Temperature Range |   | Unit |
|----------------------|----------------------------|-----------------------------|---|------|
| T <sub>J</sub>       | Junction Temperature Range | −40 °C to 135 °C            |   | °C   |
| Speed grade          | —                          | −1                          | — | —    |
| t <sub>PAGEPGM</sub> | eNVM Page Programming Time | 40                          | — | ms   |

### 6.2 Crystal Oscillator

The following tables describe the electrical characteristics of the crystal oscillator in the IGLOO 2 FPGAs.

**TABLE 6-3: ELECTRICAL CHARACTERISTICS OF THE CRYSTAL OSCILLATOR – HIGH GAIN MODE (20 MHZ)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS: T<sub>J</sub> = 135 °C, VDD = 1.14V**

| Parameter  | Description  | Min       | Typ   | Max       | Units |
|------------|--|-----------|-------|-----------|-------|
| FXTAL      | Operating frequency                                    | —         | 20    | —         | MHz   |
| ACCTXTAL   | Accuracy   | —         | —     | 0.008     | %     |
| CYCXTAL    | Output duty cycle                                      | —         | 49–51 | 47–53     | %     |
| JITPERXTAL | Output Period Jitter (peak to peak)                    | —         | 200   | 460       | ps    |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak)            | —         | 200   | 850       | ps    |
| IDYNXTAL   | Operating current                                      | —         | 1.5   | —         | mA    |
| VIHXTAL    | Input logic level High                                 | 0.9 × VPP | —     | —         | V     |
| VILXTAL    | Input logic level Low                                  | —         | —     | 0.1 × VPP | V     |
| SUXTAL     | Startup time (with regard to stable oscillator output) | —         | —     | 1.2       | ms    |

**TABLE 6-4: ELECTRICAL CHARACTERISTICS OF THE CRYSTAL OSCILLATOR – MEDIUM GAIN MODE (2 MHZ)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS: T<sub>J</sub> = 135 °C, VDD = 1.14V**

| Parameter  | Description                                 | Min | Typ   | Max   | Units |
|------------|---|-----|-------|-------|-------|
| FXTAL      | Operating frequency                         | —   | 2     | —     | MHz   |
| ACCTXTAL   | Accuracy                                    | —   | —     | 0.003 | %     |
| CYCXTAL    | Output duty cycle                           | —   | 49–51 | 46–54 | %     |
| JITPERXTAL | Output Period Jitter (peak to peak)         | —   | 1     | 5     | ns    |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | —   | 1     | 5     | ns    |

**TABLE 6-4: ELECTRICAL CHARACTERISTICS OF THE CRYSTAL OSCILLATOR – MEDIUM GAIN MODE (2 MHZ)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

| Parameter | Description  | Min              | Typ | Max              | Units |
|-----------|--|------------------|-----|------------------|-------|
| IDYNXTAL  | Operating current                                      | —                | 0.3 | —                | mA    |
| VIHXTAL   | Input logic level High                                 | $0.9 \times VPP$ | —   | —                | V     |
| VILXTAL   | Input logic level Low                                  | —                | —   | $0.1 \times VPP$ | V     |
| SUXTAL    | Startup time (with regard to stable oscillator output) | —                | —   | 9                | ms    |

**TABLE 6-5: ELECTRICAL CHARACTERISTICS OF THE CRYSTAL OSCILLATOR – LOW GAIN MODE (32 KHZ)—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter  | Description  | Min              | Typ   | Max              | Units |
|------------|--|------------------|-------|------------------|-------|
| FXTAL      | Operating frequency                                    | —                | 32    | —                | kHz   |
| ACCTXTAL   | Accuracy   | —                | —     | 0.009            | %     |
| CYCXTAL    | Output duty cycle                                      | —                | 49–51 | 44–56            | %     |
| JITPERXTAL | Output Period Jitter (peak to peak)                    | —                | 150   | 300              | ns    |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak)            | —                | 150   | 300              | ns    |
| IDYNXTAL   | Operating current                                      | —                | 0.044 | —                | mA    |
| VIHXTAL    | Input logic level High                                 | $0.9 \times VPP$ | —     | —                | V     |
| VILXTAL    | Input logic level Low                                  | —                | —     | $0.1 \times VPP$ | V     |
| SUXTAL     | Startup time (with regard to stable oscillator output) | —                | —     | 152              | ms    |

### 6.3 On-Chip Oscillator

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO 2 FPGAs.

**TABLE 6-6: ELECTRICAL CHARACTERISTICS OF THE 50 MHZ RC OSCILLATOR—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter | Description                  | Condition             | Min | Typ   | Max   | Units |
|-----------|------------------------------|-----------------------|-----|-------|-------|-------|
| F50RC     | Operating frequency          | —                     | —   | 50    | —     | MHz   |
| AC50RC    | Accuracy                     | —                     | —   | 1     | 10    | %     |
| CYC50RC   | Output duty cycle            | —                     | —   | 49–51 | 46–54 | %     |
| JIT50RC   | Output jitter (peak to peak) | Period Jitter         | —   | 200   | 550   | ps    |
|           |                              | Cycle-to-Cycle Jitter | —   | 320   | 930   | ps    |
| IDYN50RC  | Operating current            | —                     | —   | 8.5   | —     | mA    |

**TABLE 6-7: ELECTRICAL CHARACTERISTICS OF THE 1 MHZ RC OSCILLATOR—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter | Description         | Condition | Min | Typ   | Max       | Units |
|-----------|---------------------|-----------|-----|-------|-----------|-------|
| F1RC      | Operating frequency | —         | —   | 1     | —         | MHz   |
| AC1RC     | Accuracy            | —         | —   | 1     | 7         | %     |
| CYC1RC    | Output duty cycle   | —         | —   | 49–51 | 46.5–53.5 | %     |

**TABLE 6-7: ELECTRICAL CHARACTERISTICS OF THE 1 MHZ RC OSCILLATOR—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$  (CONTINUED)**

|         |                              |                       |   |     |    |    |
|---------|------------------------------|-----------------------|---|-----|----|----|
| JIT1RC  | Output jitter (peak to peak) | Period Jitter         | — | 10  | 36 | ps |
|         |                              | Cycle-to-Cycle Jitter | — | 10  | 50 | ps |
| IDYN1RC | Operating current            | —                     | — | 0.1 | —  | mA |
| SU1RC   | Startup time                 | —                     | — | —   | 24 | μs |

#### 6.4 Clock Conditioning Circuits (CCC)

The following tables list the CCC characteristics of the IGLOO 2 FPGAs.

**TABLE 6-8: IGLOO® 2 FPGAS CCC/PLL SPECIFICATION—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter  | Conditions                                      | Min   | Typ | Max  | Units | Notes |
|--|---|-------|-----|------|-------|-------|
| Clock conditioning circuitry input frequency $f_{IN\_CCC}$     | All CCC   | 1     | —   | 200  | MHz   | —     |
|  | 32 kHz Capable CCC                              | 0.032 | —   | 200  | MHz   | —     |
| Clock conditioning circuitry output frequency $f_{OUT\_CCC}$   | —   | 0.078 | —   | 400  | MHz   | 1     |
| PLL VCO frequency  | —   | 500   | —   | 1000 | MHz   | 2     |
| Delay increments in programmable delay blocks                  | —   | —     | 75  | 100  | ps    | —     |
| Number of programmable values in each programmable delay block | —   | —     | —   | 64   | —     | —     |
| Acquisition time   | $f_{IN} \geq 1 \text{ MHz}$                     | —     | 70  | 100  | μs    | —     |
|  | $f_{IN} = 32 \text{ kHz}$                       | —     | 1   | 16   | ms    | —     |
| Input duty cycle (Reference Clock)                             | <b>Internal Feedback</b>                        |       |     |      |       |       |
|  | 1 MHz $\leq f_{IN\_CCC} \leq 25 \text{ MHz}$    | 10    | —   | 90   | %     | —     |
|  | 25 MHz $\leq f_{IN\_CCC} \leq 100 \text{ MHz}$  | 25    | —   | 75   | %     | —     |
|  | 100 MHz $\leq f_{IN\_CCC} \leq 150 \text{ MHz}$ | 35    | —   | 65   | %     | —     |
|  | 150 MHz $\leq f_{IN\_CCC} \leq 200 \text{ MHz}$ | 45    | —   | 55   | %     | —     |
|  | <b>External Feedback (CCC, FPGA, Off-chip)</b>  |       |     |      |       |       |
|  | 1 MHz $\leq f_{IN\_CCC} \leq 25 \text{ MHz}$    | 25    | —   | 75   | %     | —     |
|  | 25 MHz $\leq f_{IN\_CCC} \leq 35 \text{ MHz}$   | 35    | —   | 65   | %     | —     |
|  | 35 MHz $\leq f_{IN\_CCC} \leq 50 \text{ MHz}$   | 45    | —   | 55   | %     | —     |
| Output duty cycle  | 005, 010, and 025 Devices                       | 46    | —   | 52   | %     | —     |
|  | 060 and 090 Devices                             | 44    | —   | 52   | %     | —     |
| <b>Spread Spectrum Characteristics</b>                         |   |       |     |      |       |       |
| Modulation frequency range                                     | —   | 25    | 35  | 50   | kHz   | —     |
| Modulation depth range   | —   | 0     | —   | 1.5  | %     | —     |
| Modulation depth control                                       | —   | —     | 0.5 | —    | %     | —     |

**Note 1:** The minimum output clock frequency is limited by the PLL. For more information see the [UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide](#).

**2:** The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.

**TABLE 6-9: IGLOO® 2 FPGAS CCC/PLL JITTER SPECIFICATIONS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Parameter   | Conditions/Package Combinations              |                |            |            |  |     | Units | Notes |  |  |  |  |
|---|--|----------------|------------|------------|--|-----|-------|-------|--|--|--|--|
| CCC Output Peak-to-Peak Period Jitter $f_{\text{OUT\_CCC}}$ |  |                |            |            |  |     |       |       |  |  |  |  |
| 010 FGG484 Packages   | SSO = 0                                      | 0 < SSO<br>≤ 2 | SSO<br>≤ 4 | SSO<br>≤ 8 | SSO<br>≤ 16                                  | —   | —     | *     |  |  |  |  |
| 20 MHz to 100 MHz   | Max(110, ± 1% x (1/ $f_{\text{OUT\_CCC}}$ )) |                |            |            | Max(150, ± 1% x (1/ $f_{\text{OUT\_CCC}}$ )) |     |       | ps    |  |  |  |  |
| 100 MHz to 400 MHz  | 120  | 150            |            |            |  | 170 | ps    | —     |  |  |  |  |
| 025 FGG484 Package  | 0 < SSO ≤ 16                                 |                |            |            |  |     | —     | *     |  |  |  |  |
| 20 MHz to 74 MHz  | ± 1% x (1/ $f_{\text{OUT\_CCC}}$ )           |                |            |            |  |     | ps    | —     |  |  |  |  |
| 74 MHz to 400 MHz   | 210  |                |            |            |  |     | ps    | —     |  |  |  |  |
| 005 FGG484 Package  | 0 < SSO ≤ 16                                 |                |            |            |  |     | —     | *     |  |  |  |  |
| 20 MHz to 53 MHz  | ± 1% x (1/ $f_{\text{OUT\_CCC}}$ )           |                |            |            |  |     | ps    | —     |  |  |  |  |
| 53 MHz to 400 MHz   | 270  |                |            |            |  |     | ps    | —     |  |  |  |  |
| 060 FG676 Package   | 0 < SSO ≤ 16                                 |                |            |            |  |     | —     | *     |  |  |  |  |
| 20 MHz to 100 MHz   | ± 1% x (1/ $f_{\text{OUT\_CCC}}$ )           |                |            |            |  |     | ps    | —     |  |  |  |  |
| 100 MHz to 400 MHz  | 150  |                |            |            |  |     | ps    | —     |  |  |  |  |
| 090 FGG484 and FGG676                                       | 0 < SSO ≤ 16                                 |                |            |            |  |     | —     | *     |  |  |  |  |
| 20 MHz to 100 MHz   | ± 1% x (1/ $f_{\text{OUT\_CCC}}$ )           |                |            |            |  |     | ps    | —     |  |  |  |  |
| 100 MHz to 400 MHz  | 150  |                |            |            |  |     | ps    | —     |  |  |  |  |

Note: \*SSO Data is based on LVCMOS 2.5V MSIO and/or MSIOD Bank I/Os.

**TABLE 6-10: PROGRAMMING TIMES—TYPICAL AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 25^\circ\text{C}$ ,  $VDD = 1.2\text{V}$**

|             | Device  | Image Size Bytes | JTAG    |        | 2 Step IAP |        | MSS/Cortex-M3 ISP (SmartFusion2 Only) |        | Auto Program | Auto Update | Program Recovery |       |
|-------------|---------|------------------|---------|--------|------------|--------|---------------------------------------|--------|--------------|-------------|------------------|-------|
|             |         |                  | Program | Verify | Program    | Verify | Program                               | Verify |              |             |                  |       |
| Fabric Only | M2GL005 | 302672           | 22      | 10     | 4          | 17     | 6                                     | 6      | 19           | 8           | 47               | 28    |
|             | M2GL010 | 568784           | 28      | 18     | 7          | 23     | 12                                    | 10     | 26           | 14          | 77               | 35    |
|             | M2GL025 | 1223504          | 51      | 26     | 14         | 33     | 23                                    | 21     | 39           | 29          | 150              | 41    |
|             | M2GL060 | 2418896          | 77      | 54     | 39         | 61     | 50                                    | 44     | 65           | 54          | 291              | 82    |
|             | M2GL090 | 3645968          | 113     | 126    | 60         | 84     | 73                                    | 66     | 90           | 79          | 427              | 108   |
|             |         |                  |         |        |            |        |                                       |        | Program      | Program     | Program          | Units |

**TABLE 6-10: PROGRAMMING TIMES—TYPICAL AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 25^{\circ}\text{C}$ , VDD = 1.2V (CONTINUED)**

|                    |         |                  | JTAG    |        | 2 Step IAP   |         |        | MSS/Cortex-M3 ISP (SmartFusion2 Only) |         |        | Auto Program | Auto Update       | Programming Recovery | Units |
|--------------------|---------|------------------|---------|--------|--------------|---------|--------|---------------------------------------|---------|--------|--------------|-------------------|----------------------|-------|
|                    | Device  | Image Size Bytes | Program | Verify | Authenticate | Program | Verify | Authenticate                          | Program | Verify | Program      | SPI CLK = 100 KHz | SPI CLK = 12.5 MHz   |       |
| Fabric + eNVM Only | M2GL005 | 137536           | 39      | 4      | 2            | 37      | 5      | 3                                     | 42      | 4      | 41           | 49                | 49                   | sec   |
|                    | M2GL010 | 274816           | 78      | 9      | 4            | 76      | 11     | 4                                     | 82      | 7      | 86           | 87                | 87                   | sec   |
|                    | M2GL025 | 274816           | 78      | 9      | 4            | 78      | 10     | 4                                     | 82      | 8      | 87           | 86                | 86                   | sec   |
|                    | M2GL060 | 268480           | 76      | 8      | 5            | 76      | 22     | 6                                     | 80      | 8      | 78           | 86                | 86                   | sec   |
|                    | M2GL090 | 544496           | 154     | 15     | 10           | 152     | 43     | 10                                    | 157     | 15     | 154          | 162               | 162                  | sec   |
|                    | M2GL005 | 439296           | 59      | 11     | 6            | 56      | 11     | 9                                     | 61      | 11     | 87           | 66                | 66                   | sec   |
|                    | M2GL010 | 842688           | 107     | 20     | 11           | 100     | 21     | 15                                    | 107     | 21     | 161          | 113               | 113                  | sec   |
|                    | M2GL025 | 1497408          | 120     | 35     | 19           | 113     | 32     | 26                                    | 121     | 35     | 229          | 121               | 121                  | sec   |
|                    | M2GL060 | 2686464          | 158     | 70     | 43           | 137     | 70     | 48                                    | 143     | 60     | 368          | 158               | 158                  | sec   |
|                    | M2GL090 | 4190208          | 266     | 147    | 68           | 236     | 115    | 75                                    | 244     | 91     | 582          | 260               | 260                  | sec   |

Note: External SPI flash part# AT25DF641-s3H is used during this measurement.

**TABLE 6-11: PROGRAMMING TIMES—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^{\circ}\text{C}$ , VDD = 1.14V**

|             |         |                  | JTAG    |        | 2 Step IAP   |         |        | MSS/Cortex-M3 ISP (SmartFusion2 Only) |         |        | Auto Program | Auto Update       | Programming Recovery | Units |
|-------------|---------|------------------|---------|--------|--------------|---------|--------|---------------------------------------|---------|--------|--------------|-------------------|----------------------|-------|
|             | Device  | Image Size Bytes | Program | Verify | Authenticate | Program | Verify | Authenticate                          | Program | Verify | Program      | SPI CLK = 100 KHz | SPI CLK = 12.5 MHz   |       |
| Fabric Only | M2GL005 | 302672           | 44      | 10     | 4            | 39      | 6      | 6                                     | 41      | 8      | 69           | 50                | 50                   | sec   |
|             | M2GL010 | 568784           | 50      | 18     | 7            | 45      | 12     | 10                                    | 48      | 14     | 99           | 57                | 57                   | sec   |
|             | M2GL025 | 1223504          | 73      | 26     | 14           | 55      | 23     | 21                                    | 61      | 29     | 150          | 63                | 63                   | sec   |
|             | M2GL060 | 2418896          | 99      | 54     | 39           | 83      | 50     | 44                                    | 87      | 54     | 313          | 104               | 104                  | sec   |
|             | M2GL090 | 3645968          | 135     | 126    | 60           | 106     | 73     | 66                                    | 112     | 79     | 449          | 130               | 130                  | sec   |

**TABLE 6-11: PROGRAMMING TIMES—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V (CONTINUED)**

|               |         |                  | JTAG    |        | 2 Step IAP   |         | MSS/Cortex-M3 ISP (SmartFusion2 Only) |              |         | Auto Programming  | Auto Update        | Programming Recovery |     |     |
|---------------|---------|------------------|---------|--------|--------------|---------|---------------------------------------|--------------|---------|-------------------|--------------------|----------------------|-----|-----|
|               | Device  | Image Size Bytes | Program | Verify | Authenticate | Program | Verify                                | Authenticate | Program | SPI CLK = 100 KHz | SPI CLK = 12.5 MHz | SPI CLK = 12.5 MHz   |     |     |
| eNVM Only     | M2GL005 | 137536           | 61      | 4      | 2            | 59      | 5                                     | 3            | 64      | 4                 | 63                 | 71                   | 71  | sec |
|               | M2GL010 | 274816           | 100     | 9      | 4            | 98      | 11                                    | 4            | 104     | 7                 | 108                | 109                  | 109 | sec |
|               | M2GL025 | 274816           | 100     | 9      | 4            | 100     | 10                                    | 4            | 104     | 8                 | 109                | 108                  | 108 | sec |
|               | M2GL060 | 268480           | 98      | 8      | 5            | 98      | 22                                    | 6            | 102     | 8                 | 100                | 108                  | 108 | sec |
|               | M2GL090 | 544496           | 176     | 15     | 10           | 174     | 43                                    | 10           | 179     | 15                | 176                | 184                  | 184 | sec |
| Fabric + eNVM | M2GL005 | 439296           | 71      | 11     | 6            | 78      | 11                                    | 9            | 83      | 11                | 109                | 88                   | 88  | sec |
|               | M2GL010 | 842688           | 129     | 20     | 11           | 122     | 21                                    | 15           | 129     | 21                | 183                | 135                  | 135 | sec |
|               | M2GL025 | 1497408          | 142     | 35     | 19           | 135     | 32                                    | 26           | 143     | 35                | 251                | 143                  | 143 | sec |
|               | M2GL060 | 2686464          | 180     | 70     | 43           | 159     | 70                                    | 48           | 165     | 60                | 390                | 180                  | 180 | sec |
|               | M2GL090 | 4190208          | 288     | 147    | 68           | 258     | 115                                   | 75           | 266     | 91                | 604                | 282                  | 282 | sec |

**Note:** External SPI flash part# AT25DF641-s3H is used during this measurement.

## 6.5 JTAG

The following tables list the JTAG characteristics of the IGLOO 2 FPGAs.

**TABLE 6-12: JTAG 1532—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Parameter     | Description                 | -1 Speed Grade |       |       |       |       | Units |
|---------------|-----------------------------|----------------|-------|-------|-------|-------|-------|
|               |                             | 005            | 010   | 025   | 060   | 090   |       |
| $t_{TCK2Q}$   | Clock to Q (data out)       | 7.71           | 7.91  | 7.95  | 8.61  | 9.21  | ns    |
| $t_{RSTB2Q}$  | Reset to Q (data out)       | 7.91           | 6.54  | 6.27  | 8.79  | 7.94  | ns    |
| $t_{DISU}$    | Test Data Input Setup Time  | -1.07          | -0.70 | -0.70 | -1.20 | -1.33 | ns    |
| $t_{DIHD}$    | Test Data Input Hold Time   | 2.43           | 2.38  | 2.47  | 2.57  | 2.71  | ns    |
| $t_{TMSSU}$   | Test Mode Select Setup Time | -0.75          | -0.86 | -1.13 | -0.99 | -1.03 | ns    |
| $t_{TMDHD}$   | Test Mode Select Hold Time  | 1.41           | 1.48  | 1.98  | 1.72  | 1.69  | ns    |
| $t_{TRSTREM}$ | ResetB Removal Time         | -0.81          | -1.1  | -1.38 | -1.24 | -0.8  | ns    |
| $t_{TRSTREC}$ | ResetB Recovery Time        | -0.81          | -1.1  | -1.38 | -1.25 | -0.8  | ns    |
| FTCKMAX       | TCK Maximum frequency       | 25             | 25    | 25    | 25    | 25    | MHz   |

## 6.6 Power-up to Functional Times

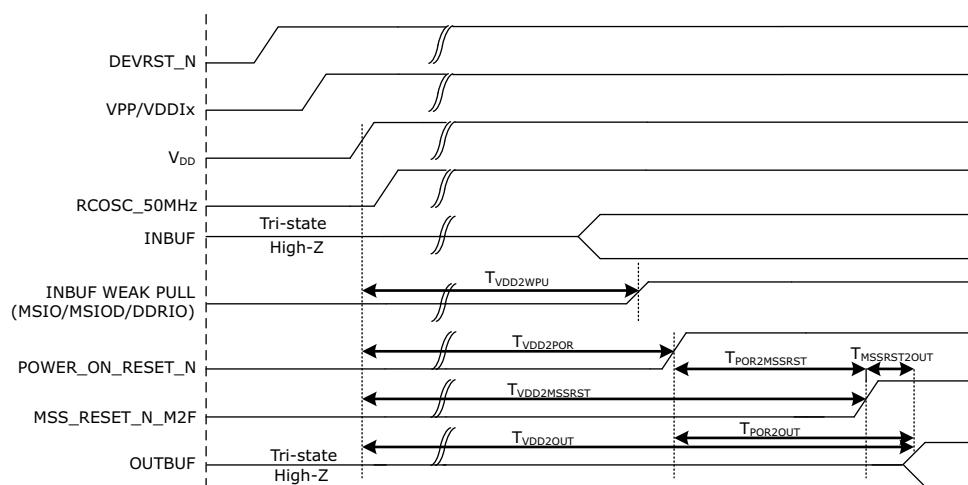
This section describes the maximum power-up to functional time in worst-case automotive Grade 1 conditions,  $T_J = 135^\circ\text{C}$ ,  $V_{DD} = 1.14\text{V}$ .

**TABLE 6-13: MAXIMUM POWER-UP TO FUNCTIONAL TIME WHEN HPMS IS USED (US)**

| Parameter        | From             | To                      | Description                                  | 005  | 010  | 025  | 060  | 090  |
|------------------|------------------|-------------------------|--|------|------|------|------|------|
| $T_{POR2OUT}$    | POWER_ON_RESET_N | Output available at I/O | Fabric to output                             | 647  | 500  | 531  | 474  | 524  |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F         | Fabric to MSS                                | 644  | 497  | 528  | 468  | 518  |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F  | Output available at I/O | MSS to output                                | 3.6  | 3.6  | 3.6  | 4.9  | 4.8  |
| $T_{VDD2OUT}$    | VDD              | Output available at I/O | VDD at its minimum threshold level to output | 3096 | 2975 | 3012 | 2869 | 2992 |
| $T_{VDD2POR}$    | VDD              | POWER_ON_RESET_N        | VDD at its minimum threshold level to Fabric | 2476 | 2487 | 2496 | 2406 | 2563 |
| $T_{VDD2MSSRST}$ | VDD              | MSS_RESET_N_M2F         | VDD at its minimum threshold level to MSS    | 3093 | 2972 | 3008 | 2864 | 2987 |
| $T_{VDD2WPU}$    | VDD              | DDRIO Inbuf Weak Pull   | VDD to Inbuf Weak Pull                       | 2500 | 2487 | 2509 | 2507 | 2519 |
|                  | VDD              | MSIO Inbuf Weak Pull    | VDD to Inbuf Weak Pull                       | 2504 | 2491 | 2510 | 2517 | 2525 |
|                  | VDD              | MSIOD Inbuf Weak Pull   | VDD to Inbuf Weak Pull                       | 2479 | 2468 | 2493 | 2486 | 2499 |

The following figure shows the power-up to functional timing diagram when HPMS is used.

**FIGURE 6-1: POWER-UP TO FUNCTIONAL TIMING DIAGRAM WHEN HPMS IS USED**



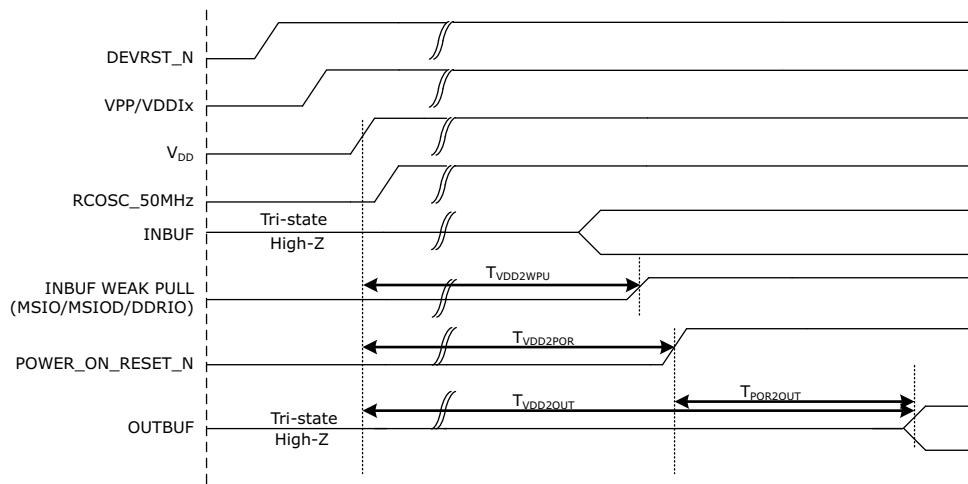
The following table lists the parameters of the power-up to functional timing diagram when HPMS is not used.

**TABLE 6-14: MAXIMUM POWER-UP TO FUNCTIONAL TIME WHEN HPMS IS NOT USED (US)**

| Parameter            | From              | To                      | Description                                  | 005  | 010  | 025  | 060  | 090  |
|----------------------|-------------------|-------------------------|--|------|------|------|------|------|
| T <sub>POR2OUT</sub> | POW-ER_ON_RESET_N | Output available at I/O | Fabric to output                             | 114  | 114  | 114  | 114  | 114  |
| T <sub>VDD2OUT</sub> | VDD               | Output available at I/O | VDD at its minimum threshold level to output | 2587 | 2600 | 2607 | 2591 | 2600 |
| T <sub>VDD2POR</sub> | VDD               | POWER_ON_RESET_N        | VDD at its minimum threshold level to Fabric | 2474 | 2486 | 2493 | 2477 | 2486 |
| T <sub>VDD2WPU</sub> | VDD               | DDRIO Inbuf Weak Pull   | VDD to Inbuf Weak Pull                       | 2500 | 2487 | 2509 | 2507 | 2519 |
|                      |                   | MSIO Inbuf Weak Pull    | VDD to Inbuf Weak Pull                       | 2504 | 2491 | 2510 | 2517 | 2525 |
|                      |                   | MSIOD Inbuf Weak Pull   | VDD to Inbuf Weak Pull                       | 2479 | 2468 | 2493 | 2486 | 2499 |

The following figure shows the power-up to functional timing diagram when HPMS is note used.

**FIGURE 6-2: POWER-UP TO FUNCTIONAL TIMING DIAGRAM WHEN HPMS IS NOT USED**



## 6.7 DEVRST\_N Characteristics

The following table lists the DEVRST\_N characteristics.

**TABLE 6-15: DEVRST\_N CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Symbol       | Description           | All Devices/Speed Grades |     |     | Units | Notes |
|--------------|-----------------------|--------------------------|-----|-----|-------|-------|
|              |                       | Min                      | Typ | Max |       |       |
| TRAMPDEVRSTN | DEVRST_N ramp time    | —                        | —   | 1   | μs    | —     |
| FMAXPDEVRSTN | DEVRST_N cycling rate | —                        | —   | 100 | kHz   | —     |

## 6.8 DEVRST\_N to Functional Times

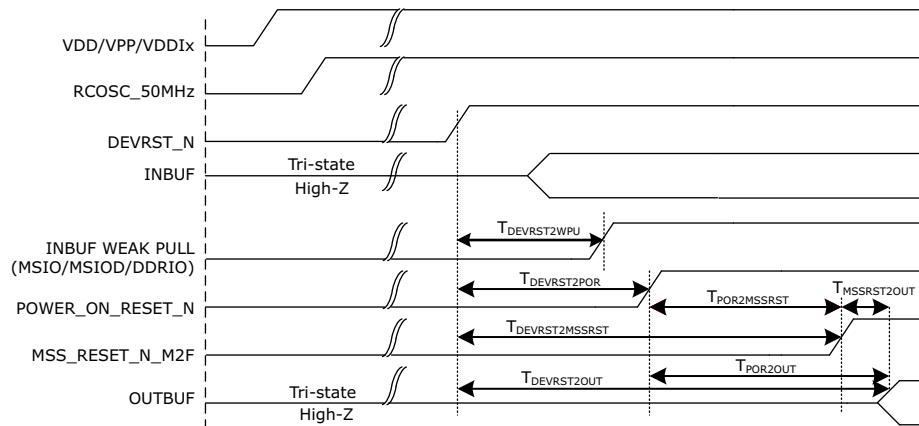
This section describes the maximum DEVRST\_N to functional time in worst-case automotive Grade 1 conditions, TJ = 135 °C, VDD = 1.14V.

**TABLE 6-16: MAXIMUM POWER-UP TO FUNCTIONAL TIME WHEN HPMS IS USED (US)**

| Parameter            | From             | To                      | Description                                  | 005 | 010 | 025 | 060 | 090 |
|----------------------|------------------|-------------------------|--|-----|-----|-----|-----|-----|
| $T_{POR2OUT}$        | POWER_ON_RESET_N | Output available at I/O | Fabric to output                             | 518 | 501 | 527 | 422 | 419 |
| $T_{POR2MSSRST}$     | POWER_ON_RESET_N | MSS_RESET_N_M2F         | Fabric to MSS                                | 515 | 497 | 524 | 417 | 414 |
| $T_{MSSRST2OUT}$     | MSS_RESET_N_M2F  | Output available at I/O | MSS to output                                | 3.5 | 3.5 | 3.5 | 4.8 | 4.8 |
| $T_{DEVRST2OUT}$     | DEVRST_N         | Output available at I/O | VDD at its minimum threshold level to output | 706 | 768 | 715 | 641 | 635 |
| $T_{DEVRST2POR}$     | DEVRST_N         | POWER_ON_RESET_N        | VDD at its minimum threshold level to Fabric | 233 | 289 | 216 | 237 | 234 |
| $T_{DEVRST2MS-SRST}$ | DEVRST_N         | MSS_RESET_N_M2F         | VDD at its minimum threshold level to MSS    | 702 | 765 | 712 | 636 | 630 |
| $T_{DEVRST2WPU}$     | DEVRST_N         | DDRIO Inbuf Weak Pull   | DEVRST_N to Inbuf Weak Pull                  | 208 | 202 | 197 | 216 | 215 |
|                      |                  | MSIO Inbuf Weak Pull    | DEVRST_N to Inbuf Weak Pull                  | 208 | 202 | 197 | 216 | 215 |
|                      |                  | MSIOD Inbuf Weak Pull   | DEVRST_N to Inbuf Weak Pull                  | 208 | 202 | 197 | 216 | 215 |

The following figure shows the DEVRST\_N to functional timing diagram when HPMS is used.

**FIGURE 6-3: DEVRST\_N TO FUNCTIONAL TIMING DIAGRAM WHEN HPMS IS USED**



The following table lists the parameters of the maximum power-up to functional time for IGLOO® 2.

**TABLE 6-17: MAXIMUM POWER-UP TO FUNCTIONAL TIME FOR IGLOO® 2 WHEN HPMS IS NOT USED (US)**

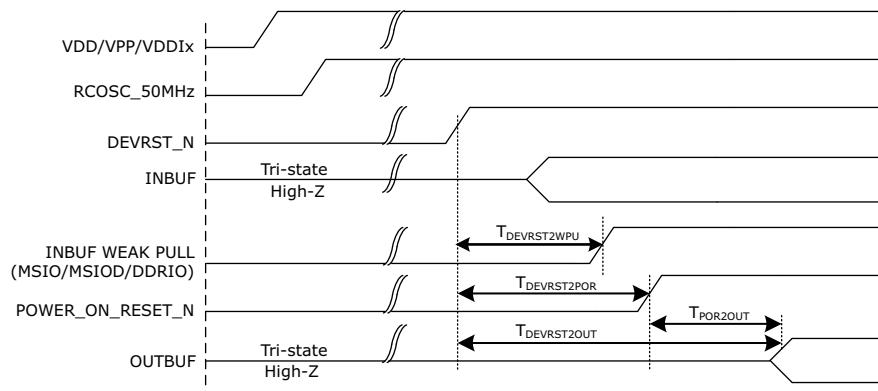
| Parameter     | From             | To                      | Description      | 005 | 010 | 025 | 060 | 090 |
|---------------|------------------|-------------------------|------------------|-----|-----|-----|-----|-----|
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 116 | 113 | 115 | 115 |

**TABLE 6-17: MAXIMUM POWER-UP TO FUNCTIONAL TIME FOR IGLOO® 2 WHEN HPMS IS NOT USED (US) (CONTINUED)**

|                  |          |                         |  |     |     |     |     |     |
|------------------|----------|-------------------------|--|-----|-----|-----|-----|-----|
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | VDD at its minimum threshold level to output | 314 | 353 | 314 | 343 | 341 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N        | VDD at its minimum threshold level to Fabric | 200 | 238 | 201 | 230 | 229 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf Weak Pull   | DEVRST_N to Inbuf Weak Pull                  | 208 | 202 | 197 | 216 | 215 |
|                  | DEVRST_N | MSIO Inbuf Weak Pull    | DEVRST_N to Inbuf Weak Pull                  | 208 | 202 | 197 | 216 | 215 |
|                  | DEVRST_N | MSIOD Inbuf Weak Pull   | DEVRST_N to Inbuf Weak Pull                  | 208 | 202 | 197 | 216 | 215 |

The following figure shows the DEVRST\_N to functional timing diagram when HPMS is not used.

**FIGURE 6-4: DEVRST\_N TO FUNCTIONAL TIMING DIAGRAM WHEN HPMS IS NOT USED**



## 6.9 System Controller SPI Characteristics

The following table lists the characteristics of the system controller SPI.

**TABLE 6-18: SYSTEM CONTROLLER SPI CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_j = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Symbol | Description                         | Conditions | All Devices/Speed Grades |     |     | Units | Notes |
|--------|-------------------------------------|------------|--------------------------|-----|-----|-------|-------|
|        |                                     |            | Min                      | Typ | Max |       |       |
| sp1    | SC_SPI_SCK minimum period           | —          | 20                       | —   | —   | ns    | —     |
| sp2    | SC_SPI_SCK minimum pulse width high | —          | 10                       | —   | —   | ns    | —     |
| sp3    | SC_SPI_SCK minimum pulse width low  | —          | 10                       | —   | —   | ns    | —     |

**Note 1:** \*For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis>. Use the supported I/O Configurations for the System Controller SPI in Table 6-19.

**2:** SC\_SPI\_SDO becomes tri-stated after SC\_SPI\_SS is de-asserted.

**TABLE 6-18: SYSTEM CONTROLLER SPI CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V (CONTINUED)**

|   |   |   |     |       |    |    |   |
|---|---|---|-----|-------|----|----|---|
| sp4   | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%) 1 | I/O Configuration: LV TTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C | —   | 1.239 | —  | ns | — |
| sp5   | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%) 1 | I/O Configuration: LV TTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C | —   | 1.245 | —  | ns | — |
| sp6   | Data from master (SC_SPI_SDO) setup time                | —   | 160 | —     | —  | ns | — |
| sp7   | Data from master (SC_SPI_SDO) hold time                 | —   | 160 | —     | —  | ns | — |
| sp8   | SC_SPI_SDI setup time                                   | —   | 20  | —     | —  | ns | — |
| sp9   | SC_SPI_SDI hold time                                    | —   | 20  | —     | —  | ns | — |
| Delay on SC_SPI_SDO after SC_SPI_SS is de-asserted when using SPI slave programming. <sup>2</sup> |   |   |     | 265   | ns | —  |   |

**Note 1:** \*For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis>. Use the supported I/O Configurations for the System Controller SPI in [Table 6-19](#).

**2:** SC\_SPI\_SDO becomes tri-stated after SC\_SPI\_SS is de-asserted.

The following table lists the supported I/O configurations for the system controller SPI.

**TABLE 6-19: SUPPORTED I/O CONFIGURATIONS FOR SYSTEM CONTROLLER SPI (FOR MSIO BANK ONLY)**

| Voltage Supply | I/O Drive Configuration | Units |
|----------------|-------------------------|-------|
| 3.3V           | 20                      | mA    |
| 2.5V           | 16                      | mA    |
| 1.8V           | 12                      | mA    |
| 1.5V           | 8                       | mA    |
| 1.2V           | 4                       | mA    |

## 6.10 Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO 2 mathblock supports 18 x 18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

**TABLE 6-20: MATHBLOCKS WITH ALL REGISTERS USED—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Mathblock With All Registers Used |                                    | Speed Grade -1 |     | Units |
|-----------------------------------|------------------------------------|----------------|-----|-------|
| Parameter                         | Description                        | Min            | Max |       |
| $t_{MISU}$                        | Input, Control Register Setup time | 0.155          | —   | ns    |
| $t_{MIHD}$                        | Input, Control Register Hold time  | 0.083          | —   | ns    |
| $t_{MOCDINSU}$                    | CDIN Input Setup time              | 1.741          | —   | ns    |
| $t_{MOCDINHD}$                    | CDIN Input Hold time               | -0.434         | —   | ns    |

**TABLE 6-20: MATHBLOCKS WITH ALL REGISTERS USED—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V (CONTINUED)**

|                 |                                     |       |       |    |
|-----------------|-------------------------------------|-------|-------|----|
| $t_{MSRSTENSU}$ | Synchronous Reset/Enable Setup time | 0.192 | —     | ns |
| $t_{MSRSTENHD}$ | Synchronous Reset/Enable Hold time  | 0.012 | —     | ns |
| $t_{MARSTREM}$  | Asynchronous Reset Removal time     | 0     | —     | ns |
| $t_{MARSTREC}$  | Asynchronous Reset Recovery time    | 0.091 | —     | ns |
| $t_{MOCQ}$      | Output Register Clock to Out delay  | —     | 0.241 | ns |
| $t_{MCLKMP}$    | CLK Minimum period                  | 2.327 | —     | ns |

**TABLE 6-21: MATHBLOCK WITH INPUT BYPASSED AND OUTPUT REGISTERS USED—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Mathblock With Input Bypassed and Output Registers Used |                                     | Speed Grade -1 |       | Units |
|---|-------------------------------------|----------------|-------|-------|
| Parameter   | Description                         | Min            | Max   |       |
| $t_{MOSU}$  | Output Register Setup time          | 2.378          | —     | ns    |
| $t_{MOHD}$  | Output Register Hold time           | -0.46          | —     | ns    |
| $t_{MOCDINSU}$  | CDIN Input Setup time               | 1.741          | —     | ns    |
| $t_{MOCDINHD}$  | CDIN Input Hold time                | -0.434         | —     | ns    |
| $t_{MSRSTENSU}$   | Synchronous Reset/Enable Setup time | 0.119          | —     | ns    |
| $t_{MSRSTENHD}$   | Synchronous Reset/Enable Hold time  | 0.012          | —     | ns    |
| $t_{MARSTREM}$  | Asynchronous Reset Removal time     | 0              | —     | ns    |
| $t_{MARSTREC}$  | Asynchronous Reset Recovery time    | 0.015          | —     | ns    |
| $t_{MOCQ}$  | Output Register Clock to Out delay  | —              | 0.241 | ns    |
| $t_{MCLKMP}$  | CLK Minimum period                  | 2.258          | —     | ns    |

**TABLE 6-22: MATHBLOCK WITH INPUT REGISTER USED AND OUTPUT IN BYPASS MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Mathblock With Input Register Used and Output in Bypass Mode |                                      | Speed Grade -1 |       | Units |
|--|--------------------------------------|----------------|-------|-------|
| Parameter  | Description                          | Min            | Max   |       |
| $t_{MISU}$   | Input Register Setup time            | 0.155          | —     | ns    |
| $t_{MIHD}$   | Input Register Hold time             | 0.083          | —     | ns    |
| $t_{MSRSTENSU}$  | Synchronous Reset/Enable Setup time  | 0.192          | —     | ns    |
| $t_{MSRSTENHD}$  | Synchronous Reset/Enable Hold time   | -0.013         | —     | ns    |
| $t_{MARSTREM}$   | Asynchronous Reset Removal time      | -0.005         | —     | ns    |
| $t_{MARSTREC}$   | Asynchronous Reset Recovery time     | 0.091          | —     | ns    |
| $t_{MICQ}$   | Input Register Clock to Output delay | —              | 2.611 | ns    |
| $t_{MCDIN2Q}$  | CDIN to Output delay                 | —              | 2.022 | ns    |

**TABLE 6-23: MATHBLOCK WITH INPUT AND OUTPUT IN BYPASS MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Mathblock With Input and Output in Bypass Mode |                       | Speed Grade -1 |       | Units |
|--|-----------------------|----------------|-------|-------|
| Parameter                                      | Description           | Min            | Max   |       |
| $t_{MIQ}$                                      | Input to Output delay | —              | 2.662 | ns    |

**TABLE 6-23: MATHBLOCK WITH INPUT AND OUTPUT IN BYPASS MODE—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V (CONTINUED)**

|               |                      |   |       |    |
|---------------|----------------------|---|-------|----|
| $t_{MCDIN2Q}$ | CDIN to Output delay | — | 2.022 | ns |
|---------------|----------------------|---|-------|----|

### 6.11 Flash\*Freeze Timing Characteristics

The following table lists the characteristics of the Flash\*Freeze entry and exit times.

**TABLE 6-24: FLASH\*FREEZE ENTRY AND EXIT TIMES—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Symbols   | Parameters                                     | Conditions  | Entry/Exit Timing<br>FCLK=100 MHz | Entry/Exit Timing<br>FCLK=3 MHz | Units | Notes |
|-----------|--|---|-----------------------------------|---------------------------------|-------|-------|
| TFF_ENTRY | Entry time                                     | eNVM and MSS/HPMS PLL = ON  | 170                               | 340                             | μs    | —     |
|           |  | eNVM and MSS/HPMS PLL = OFF   | 230                               | 460                             | μs    | —     |
| TFF_EXIT  | Exit Time with respect to MSS PLL Lock         | eNVM and MSS/HPMS PLL = ON during F*F   | 110                               | 150                             | μs    | —     |
|           |  | eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit | 150                               | 200                             | μs    | —     |
|           |  | eNVM and MSS PLL = OFF during F*F and both are turned back on at exit               | 210                               | 300                             | μs    | —     |
|           |  | eNVM = OFF and MSS PLL = ON during F*F and eNVM turned back on at exit              | 210                               | 300                             | μs    | —     |
|           | Exit Time with respect to Fabric PLL Lock      | eNVM and MSS/HPMS PLL = ON during F*F   | 1.5                               | 1.5                             | ms    | *     |
|           |  | eNVM and MSS PLL = OFF during F*F and both are turned back on at exit               | 1.5                               | 1.5                             | ms    | *     |
|           | Exit Time with respect to Fabric buffer output | eNVM and MSS/HPMS PLL = ON during F*F   | 30                                | 30                              | μs    | —     |
|           |  | eNVM and MSS PLL = OFF during F*F and both are turned back on at exit               | 70                                | 70                              | μs    | —     |

Note: \* PLL Lock Delay set to 1024 cycles (default)

### 6.12 IGLOO 2 Specifications

#### 6.13 HPMS Clock Frequency

The following table describes the maximum frequency for HPMS main clock.

**TABLE 6-25: MAXIMUM FREQUENCY FOR HPMS MAIN CLOCK—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V**

| Symbol   | Description                                      | Speed Grade<br>-1 | Units |
|----------|--|-------------------|-------|
| HPMS_CLK | Maximum Frequency for the HPMS Main Clock (FCLK) | 133               | MHz   |

## 6.14 IGLOO 2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_0\_CLK. For timing parameter definitions, see [Figure 6-5](#). The following table lists the SPI characteristics.

**TABLE 6-26: SPI CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$**

| Symbol   | Description   | All Devices/Speed Grades |       |     | Unit | Notes |
|--|---|--------------------------|-------|-----|------|-------|
|  |   | Min                      | Typ   | Max |      |       |
| SPIFMAX  | Maximum operating frequency of SPI interface                  | —                        | —     | 20  | MHz  | —     |
| sp1  | <b>SPI_[0 1]_CLK minimum period</b>                           |                          |       |     |      |       |
|  | SPI_[0 1]_CLK = PCLK/2  | 12                       | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/4  | 24.1                     | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/8  | 48.2                     | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/16                                       | 0.1                      | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/32                                       | 0.19                     | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/64                                       | 0.39                     | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/128                                      | 0.77                     | —     | —   | μs   | —     |
| sp2  | <b>SPI_[0 1]_CLK minimum pulse width high</b>                 |                          |       |     |      |       |
|  | SPI_[0 1]_CLK = PCLK/2  | 6                        | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/4  | 12.05                    | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/8  | 24.1                     | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/16                                       | 0.05                     | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/32                                       | 0.095                    | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/64                                       | 0.195                    | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/128                                      | 0.385                    | —     | —   | μs   | —     |
| sp3  | <b>SPI_[0 1]_CLK minimum pulse width low</b>                  |                          |       |     |      |       |
|  | SPI_[0 1]_CLK = PCLK/2  | 6                        | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/4  | 12.05                    | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/8  | 24.1                     | —     | —   | ns   | —     |
|  | SPI_[0 1]_CLK = PCLK/16                                       | 0.05                     | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/32                                       | 0.095                    | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/64                                       | 0.195                    | —     | —   | μs   | —     |
|  | SPI_[0 1]_CLK = PCLK/128                                      | 0.385                    | —     | —   | μs   | —     |
| sp4  | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) | —                        | 2.77  | —   | ns   | 1     |
| sp5  | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) | —                        | 2.906 | —   | ns   | 1     |
| <b>SPI Master Configuration (Applicable to 005, 010 and 025)</b> |   |                          |       |     |      |       |

**TABLE 6-26: SPI CHARACTERISTICS—WORST-CASE AUTOMOTIVE GRADE 1 CONDITIONS:  $T_J = 135^\circ\text{C}$ , VDD = 1.14V (CONTINUED)**

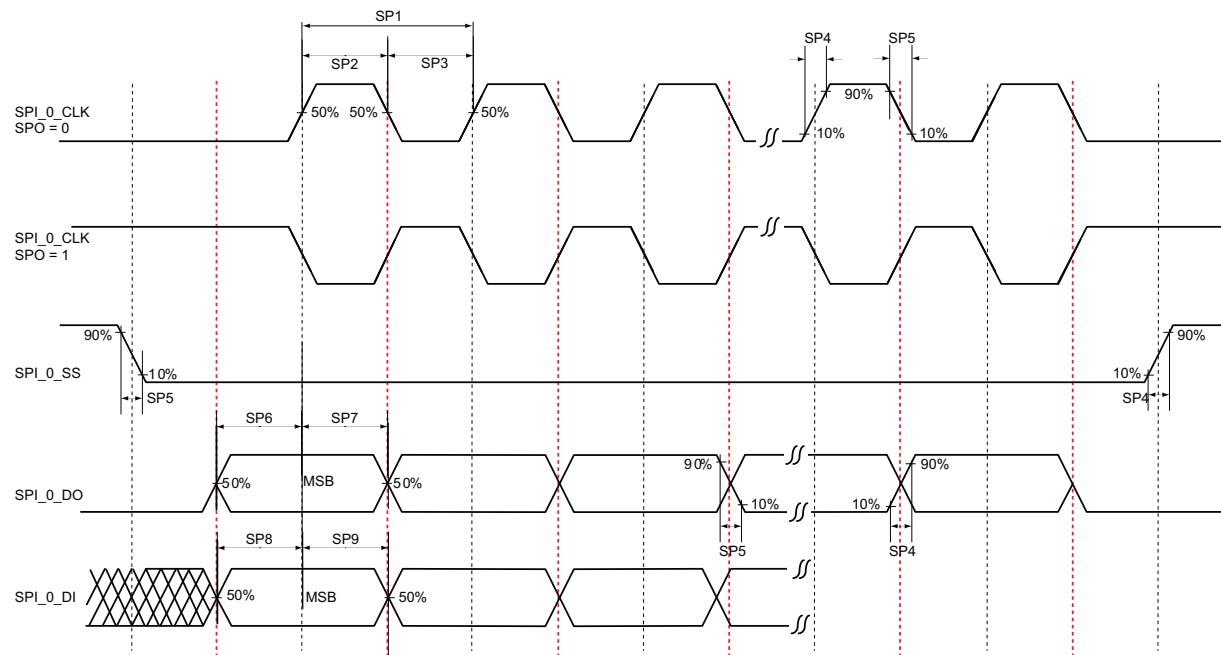
| Symbol  | Description             | All Devices/Speed Grades    |     |     | Unit | Notes |
|---|-------------------------|-----------------------------|-----|-----|------|-------|
|   |                         | Min                         | Typ | Max |      |       |
| sp6m  | SPI_[0 1]_DO setup time | (SPI_x_CLK_period/2) – 7.5  | —   | —   | ns   | 2     |
| sp7m  | SPI_[0 1]_DO hold time  | (SPI_x_CLK_period/2) – 2.5  | —   | —   | ns   | 2     |
| sp8m  | SPI_[0 1]_DI setup time | 12.5                        | —   | —   | ns   | 2     |
| sp9m  | SPI_[0 1]_DI hold time  | 2.5                         | —   | —   | ns   | 2     |
| <b>SPI Slave Configuration (Applicable to 005, 010 and 025)</b> |                         |                             |     |     |      |       |
| sp6s  | SPI_[0 1]_DO setup time | (SPI_x_CLK_period/2) – 16.5 | —   | —   | ns   | 2     |
| sp7s  | SPI_[0 1]_DO hold time  | (SPI_x_CLK_period/2) + 3.0  | —   | —   | ns   | 2     |
| sp8s  | SPI_[0 1]_DI setup time | 2                           | —   | —   | ns   | 2     |
| sp9s  | SPI_[0 1]_DI hold time  | 7.5                         | —   | —   | ns   | 2     |
| <b>SPI Master Configuration (Applicable to 060 and 090)</b>     |                         |                             |     |     |      |       |
| sp6m  | SPI_[0 1]_DO setup time | (SPI_x_CLK_period/2) – 6.5  | —   | —   | ns   | 2     |
| sp7m  | SPI_[0 1]_DO hold time  | (SPI_x_CLK_period/2) – 9    | —   | —   | ns   | 2     |
| sp8m  | SPI_[0 1]_DI setup time | 15.5                        | —   | —   | ns   | 2     |
| sp9m  | SPI_[0 1]_DI hold time  | -2                          | —   | —   | ns   | 2     |
| <b>SPI Slave Configuration (Applicable to 060 and 090)</b>      |                         |                             |     |     |      |       |
| sp6s  | SPI_[0 1]_DO setup time | (SPI_x_CLK_period/2) – 15.5 | —   | —   | ns   | 2     |
| sp7s  | SPI_[0 1]_DO hold time  | (SPI_x_CLK_period/2) – 3    | —   | —   | ns   | 2     |
| sp8s  | SPI_[0 1]_DI setup time | 3.5                         | —   | —   | ns   | 2     |
| sp9s  | SPI_[0 1]_DI hold time  | 3                           | —   | —   | ns   | 2     |

**Note 1:** For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website:  
<https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis>.

**2:** For allowable pclk configurations, see the Serial Peripheral Interface Controller section in the [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

The following figure shows the SPI timing diagram.

**FIGURE 6-5: SPI TIMING FOR A SINGLE FRAME TRANSFER IN MOTOROLA MODE (SPH = 1)**



## 6.15 SRAM PUF

This section describes the on-static random-access memory (SRAM) physical unclonable functions (PUF) in worst-case automotive Grade 1 conditions,  $T_J = 135^\circ\text{C}$ ,  $VDD = 1.14\text{V}$ . For more information about SRAM PUF services, see [AC434: Using SRAM PUF System Service in SmartFusion2 Application Note](#).

**TABLE 6-27: SRAM PUF**

| Service                  | PUF Off |         | PUF On |         | Units |
|--------------------------|---------|---------|--------|---------|-------|
|                          | Typ     | Max     | Typ    | Max     |       |
| Create Activation Code   | 709.1   | 787.9   | 796.0  | 884.5   | ms    |
| Delete Activation Code   | 1329.3  | 1477.0  | 1303.0 | 1447.7  | ms    |
| Create Intrinsic KeyCode | 656.6   | 729.5   | 643.6  | 715.1   | ms    |
| Create Extrinsic KeyCode | 656.6   | 729.5   | 643.6  | 715.1   | ms    |
| Get Number of Keys       | 1.3     | 1.5     | 1.3    | 1.5     | ms    |
| Export (KC0, KC1)        | 998.0   | 1108.9  | 978.2  | 1086.9  | ms    |
| Export 2 KeyCodes        | 2020.2  | 2244.7  | 1980.2 | 2200.2  | ms    |
| Export 4 KeyCodes        | 3065.7  | 3406.3  | 3005.0 | 3338.8  | ms    |
| Export 8 KeyCodes        | 5101.0  | 5667.8  | 5000.0 | 5555.6  | ms    |
| Export 16 KeyCodes       | 9212.1  | 10235.7 | 9029.7 | 10033.0 | ms    |
| Import (KC0, KC1)        | 39.7    | 44.1    | 38.9   | 43.2    | ms    |
| Import 2 KeyCodes        | 50.1    | 55.7    | 49.1   | 54.6    | ms    |
| Import 4 KeyCodes        | 60.6    | 67.3    | 59.4   | 66.0    | ms    |
| Import 8 KeyCodes        | 80.9    | 89.9    | 79.3   | 88.1    | ms    |
| Import 16 KeyCodes       | 123.8   | 137.6   | 121.4  | 134.9   | ms    |
| Delete KeyCode           | 552.5   | 613.9   | 541.6  | 601.8   | ms    |
| Fetch Key                | 31.4    | 34.8    | 11.5   | 12.8    | ms    |
| Fetch ECC Key            | 20.0    | 22.2    | 1.9    | 2.1     | ms    |
| Get Seed                 | 2.0     | 2.3     | 0.9    | 1.0     | ms    |

## 6.16 Non-deterministic Random Bit Generator Characteristics

This section describes the NRBG characteristics in worst-case automotive Grade 1 conditions,  $T_J = 135 \text{ }^{\circ}\text{C}$ ,  $VDD = 1.14\text{V}$ . For more information about NRBG, see [AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note](#).

**TABLE 6-28: NON-DETERMINISTIC RANDOM BIT GENERATOR CHARACTERISTICS**

| Service                         | Conditions                |                  | Timing                              | Units | Notes |
|---------------------------------|---------------------------|------------------|-------------------------------------|-------|-------|
|                                 | Prediction Resistance     | Additional Input |                                     |       |       |
| Instantiate                     | OFF                       | X                | 85                                  | ms    | —     |
| Generate<br>(after Instantiate) | OFF                       | 0                | 4.5 ms + (7 us/byte x No. of Bytes) | —     | 1     |
|                                 | OFF                       | 64               | 6.0 ms + (7 us/byte x No. of Bytes) | —     |       |
|                                 | OFF                       | 128              | 7.0 ms + (7 us/byte x No. of Bytes) | —     |       |
|                                 | ON                        | X                | 47                                  | ms    | 1     |
| Generate<br>(subsequent)        | OFF                       | 0                | 0.5 ms + (7 us/byte x No. of Bytes) | —     | —     |
|                                 | OFF                       | 64               | 2.0 ms + (7 us/byte x No. of Bytes) | —     |       |
|                                 | OFF                       | 128              | 3.0 ms + (7 us/byte x No. of Bytes) | —     | —     |
|                                 | ON                        | X                | 43                                  | ms    | —     |
| Reseed                          | —                         | —                | 40                                  | ms    | —     |
| Uninstantiate                   | —                         | —                | 0.16                                | ms    | —     |
| Reset                           | —                         | —                | 0.10                                | ms    | —     |
| Self Test                       | First time after power up |                  | 20                                  | ms    | —     |
|                                 | Subsequent                |                  | 6                                   | ms    | —     |

1: If PUF\_OFF, generate would incur additional PUF Delay time for consecutive service calls.

## 6.17 Cryptographic Block Characteristics

This section describes the Cryptographic block characteristics in worst-case automotive Grade 1 conditions,  $T_J = 135 \text{ }^{\circ}\text{C}$ ,  $VDD = 1.14\text{V}$ . For more information about Cryptographic block and associated services, see [AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note](#) and [AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note](#).

**TABLE 6-29: CRYPTOGRAPHIC BLOCK CHARACTERISTICS**

| Service                                       | Conditions                              | Timing | Units |
|---|---|--------|-------|
| Any Service                                   | First certificate check penalty at boot | 11.5   | ms    |
| AES128/256 (Encoding / Decoding) <sup>1</sup> | Up to 100 blocks                        | 170    | kbps  |
|   | 100 blocks up to 64k blocks             | 630    | kbsps |
| SHA256  | 512 bits                                | 520    | kbsps |
|   | 1024 bits                               | 760    | kbsps |
|   | 2048 bits                               | 930    | kbsps |
|   | 24 kbytes                               | 1110   | kbsps |
| HMAC  | 512 bytes                               | 800    | kbsps |
|   | 1024 bytes                              | 870    | kbsps |
|   | 2048 bytes                              | 900    | kbsps |
|   | 24 kbytes                               | 950    | kbsps |
| KeyTree                                       | —                                       | 1.78   | ms    |
| Challenge-Response                            | PUF = OFF                               | 24.6   | ms    |
|   | PUF = ON                                | 7      | ms    |

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**TABLE 6-29: CRYPTOGRAPHIC BLOCK CHARACTERISTICS (CONTINUED)**

| <b>Service</b>           | <b>Conditions</b> | <b>Timing</b> | <b>Units</b> |
|--------------------------|-------------------|---------------|--------------|
| ECC Point Multiplication | —                 | 603           | ms           |
| ECC Point Addition       | —                 | 8             | ms           |

**Note 1:** Using Cypher Block Chaining (CBC) mode.

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## APPENDIX A: REVISION HISTORY

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the latest publication.

### A.1 Revision A - 01/2023

The following is a summary of changes in revision A of the document:

- The document was migrated to Microchip template.
- The document number was updated from DS0138 to DS50003504A.
- Updated the value of “Access Time with Feed-Through Write Timing” in [Table 5-1](#), [Table 5-2](#), [Table 5-3](#), [Table 5-4](#), and [Table 5-5](#). For more information about this change, see [https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/can/CN\\_SF2\\_IGLOO2\\_FPGA\\_LSRAM\\_Write-Feedthrough\\_Timing.pdf](https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/can/CN_SF2_IGLOO2_FPGA_LSRAM_Write-Feedthrough_Timing.pdf)
- Updated the value under the “Auto Update” column in [Table 6-10](#) and [Table 6-11](#).
- Updated [Table 6-18](#) by inserting a row below the Sp9 row and adding a note.

### A.2 Revision 3 - 09/2018

The following is a summary of changes in revision 3 of the document:

- Information about DEVRSTN ramp time was updated. See [Table 6-15](#).

The following information was added in revision 3.0 of this document.

- A note about VID was added to LVDS differential voltage specification. See [Table 2-57](#).

### A.3 Revision 2 - 05/2018

The following is a summary of changes in revision 2 of the document:

The following information was updated in revision 2.0 of this document.

- High temperature data retention. See [Table 1-6](#) and [Figure 1-1](#).
- Input capacitance and leakage current. See [Table 2-3](#).
- Listed 060 device for output duty cycle in CCC/PLL specification. See [Table 6-8](#).
- Speed grade -1 was updated for Register Delays, Combinatorial Cell Propagation Delays, Input Data Register Propagation Delays, Output/Enable Data Register Propagation Delays, Input DDR Propagation Delays, and Output DDR Propagation Delays. See [Table 3-2](#), [Table 3-1](#), [Table 2-82](#), [Table 2-83](#), [Table 2-84](#), and [Table 2-85](#).
- Power-up. See [Section 6.6, Power-up to Functional Times](#).
- DEVRST\_N. See [Section 6.8, DEVRST\\_N to Functional Times](#).
- SRAM PUF. See [Table 6-27](#).
- Non-deterministic Random Bit Generator (NRBG) Characteristics. See [Table 6-28](#).
- Cryptographic block characteristics. See [Table 6-29](#).

### A.4 Revision 1 - 06/2015

This is the initial revision of this document.

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